Математические модели и методы синтеза СБИС

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Содержание

- ✓ Задача синтеза интегральных схем и основные сведения о КМОП технологии
- Задача разбиения электрической схемы
- Задача размещения модулей СБИС
- Задача трассировки соединений

Литература

1. Sima Dimitrijev, « Understanding Semiconductor Devices », Oxford University Press, 2000.
2. Behzad Razavi, « Design of Analog CMOS Integrated Circuits », McGraw-Hill, 2001.
3. Yuan Taur, and Tak H. Ning, « Fundamentals of Modern VLSI Devices », Cambridge University Press, 2000.
4. Etienne Sicard, « Introduction to Microwind2 ».
5. Mohamed Dessouky, « Analog design classes ».
6. International Technology Roadmap for Semiconductors, ITRS Reports. http://www.itrs.net/reports.html

CMOS Process

- Most popular technology for realizing microcircuits.
- Lower fabrication **cost.**
- Scaling: Easy to reduce **dimensions.**
- **In digital circuits** CMOS consumes less power and requires fewer devices than BJT.
- **In analog**, the MOST is slower and noisier than the BJT. However, the speed of MOST is continuously increasing and becoming comparable to BJT's.

Silicon

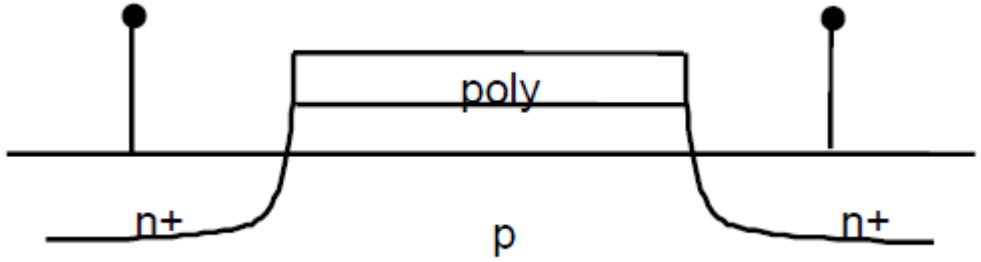
IC fabrication depends on two properties of silicon:

- It is a semiconductor
  - Conductivity can be changed by adding impurities
  - These impurities, called dopants, can create either n-type or p-type regions.
- Its oxide is very stable
  - It is SiO_2, which is quartz or glass (amorphous)
  - Great for sealing stuff from impurities
  - Can be selectively patterned.
  - Etching can remove SiO_2 without harming Si.
  - Stable grown oxide is the great advantage of Si over Ge or GaAs.

Doping

- Adding **arsenic** or phosphorous to the intrinsic silicon increases its conductivity by adding ‘free’ electrons. Silicon with electron carriers is called n-type silicon, since the current is carried by particles with negative charge.
- Adding **boron** to intrinsic silicon increases its conductivity by adding ‘free’ holes. Holes are like electrons, but have a positive charge, so this type of material is called p-type silicon.

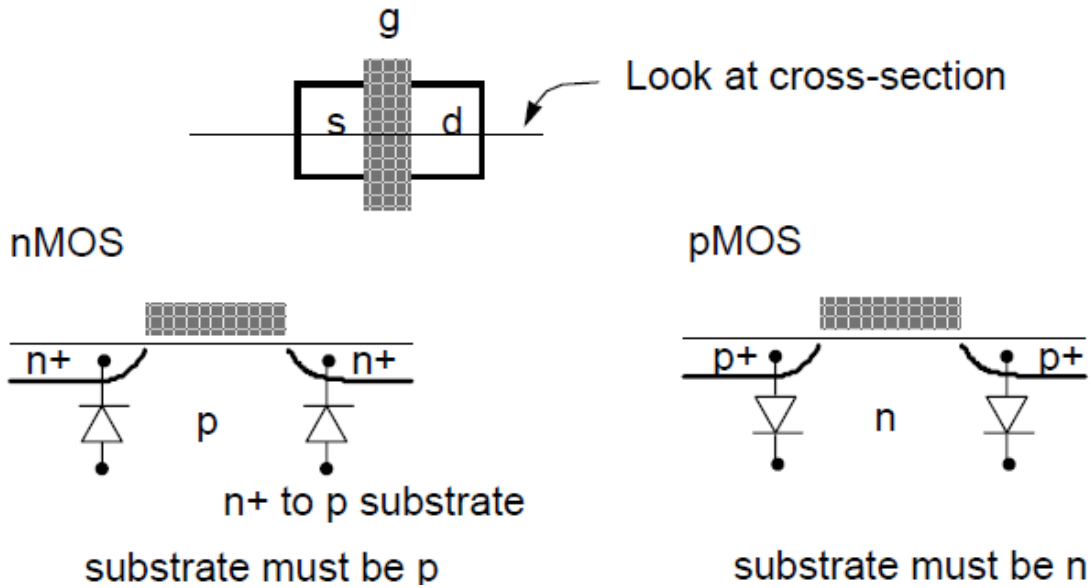
How to Build a Transistor



Diffusion is made by adding impurities into the silicon

- n+(p+) diffusion means the region has a lot of impurities which improves it conductivity
- p (n) regions are more lightly doped
- p region is formed first, and then the n+ over dope parts of the p region to form the n+ regions
- n+ dopant is added after the poly is down so poly blocks dopants

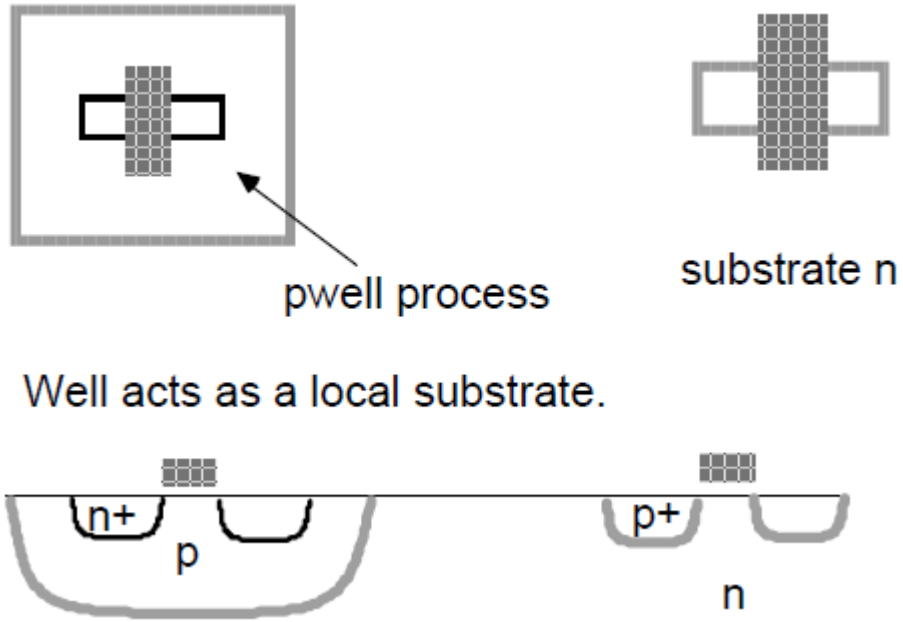
CMOS Has Two Transistor Types



CMOS devices require two types of substrates:

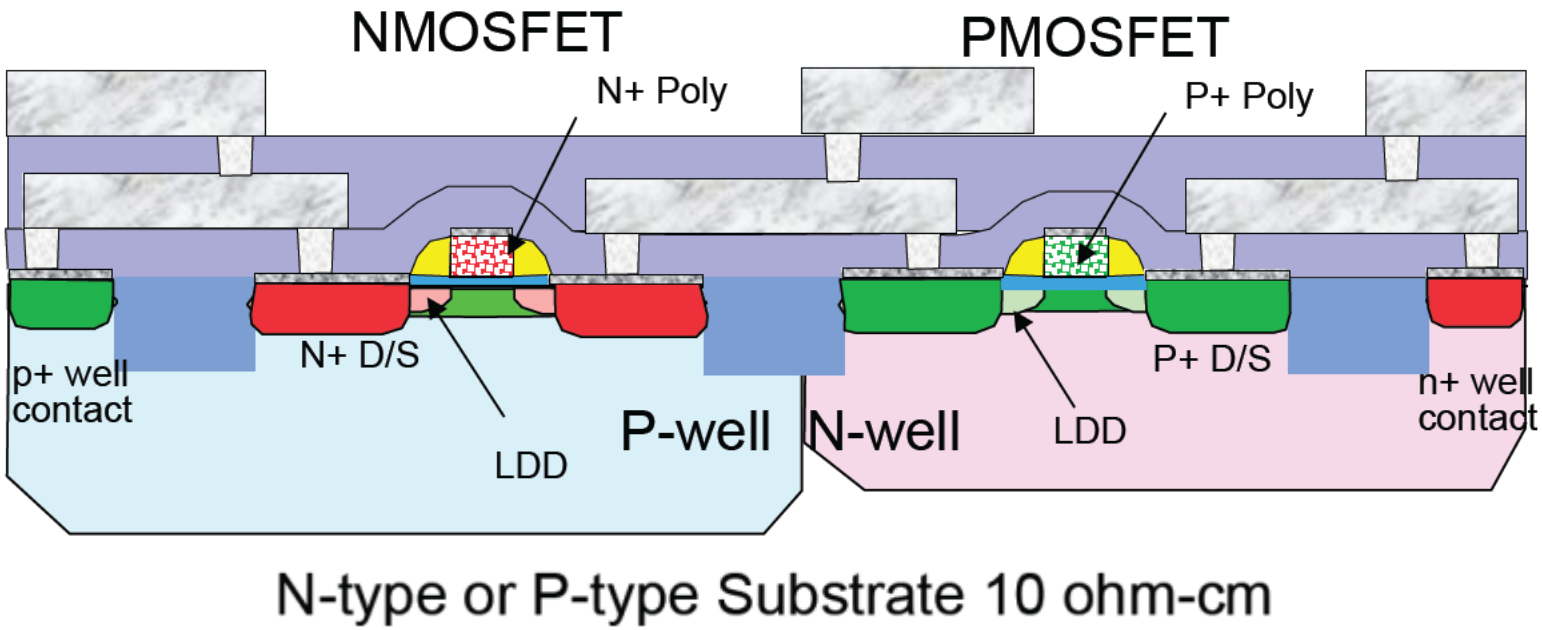
- n-type for pMOS
- p-type for nMOS

Wells: Local Substrates



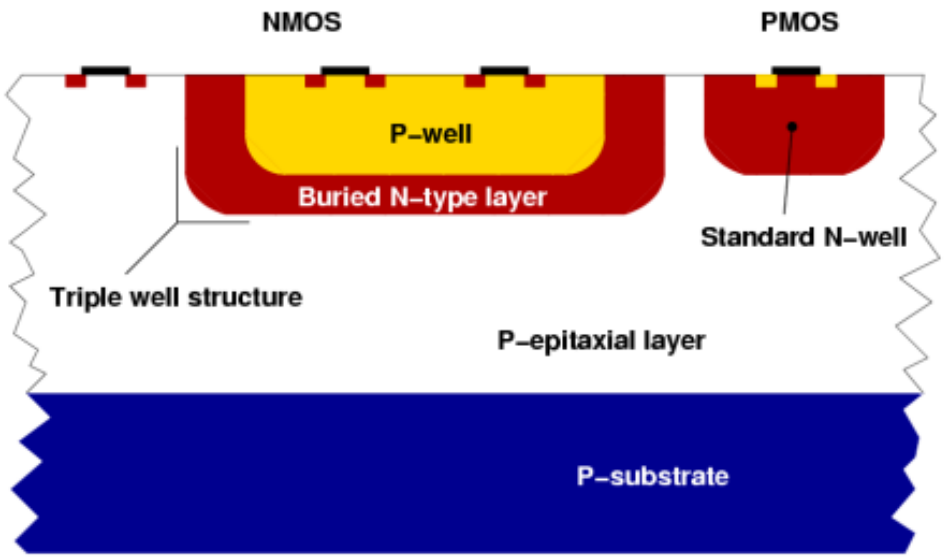
- Fabricators can choose to make the base wafer n-type (add pwells) or p-type (add nwells), or choose to add both, ("twin"wells).

Twin-Well Process



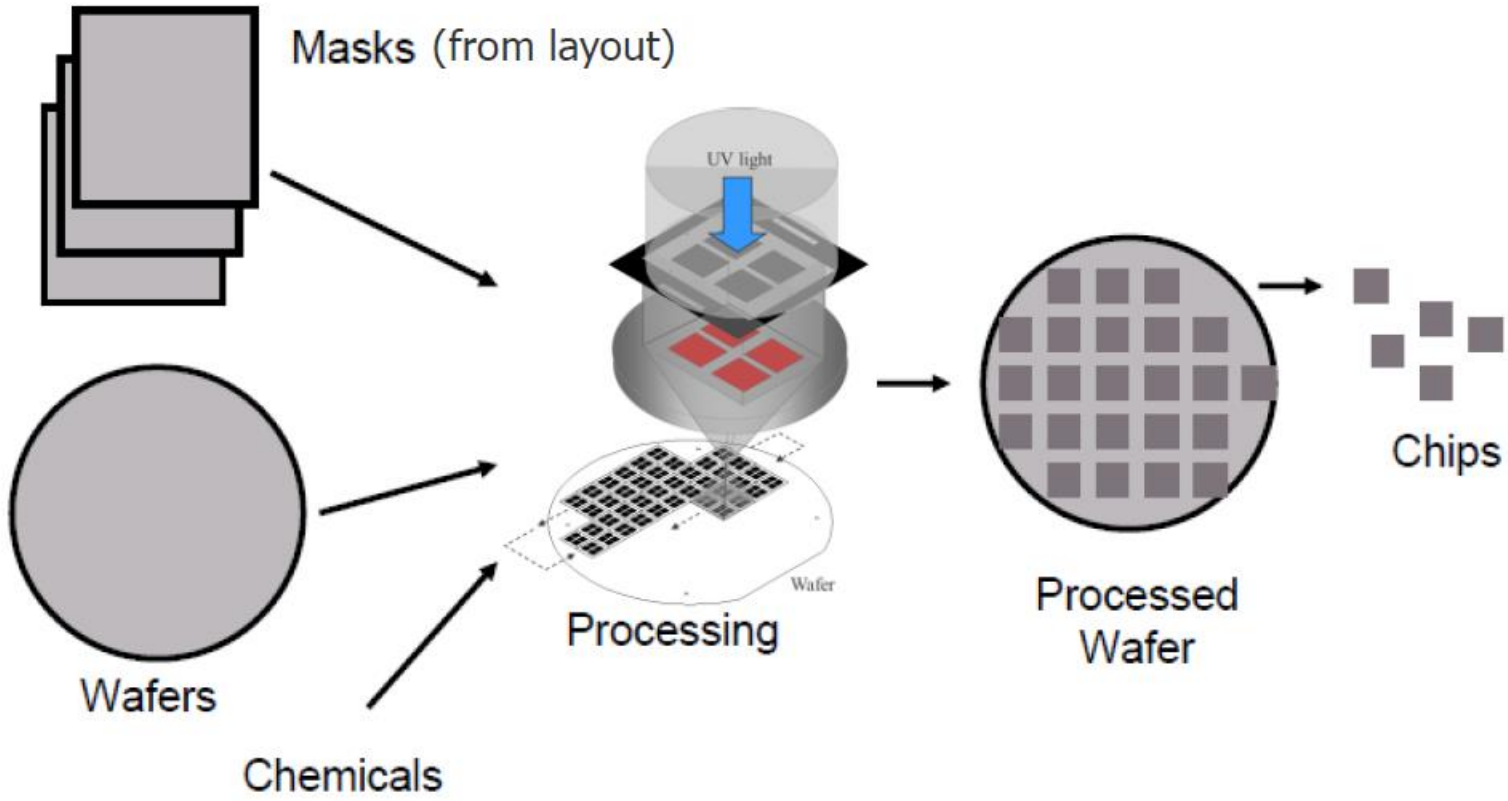
- Two wells may exist (PWELL & NWELL) called twin-tub process.
- Allows both wells to be optimally doped.

Triple-Well Process



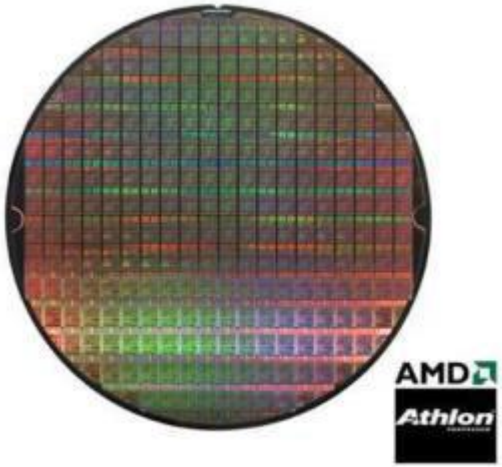
- In triple-well CMOS processes a deep n-well is used as a shielding frame against disturbance from the substrate to provide N-channel MOSFETs with better isolation from substrate noise.

Making Chips

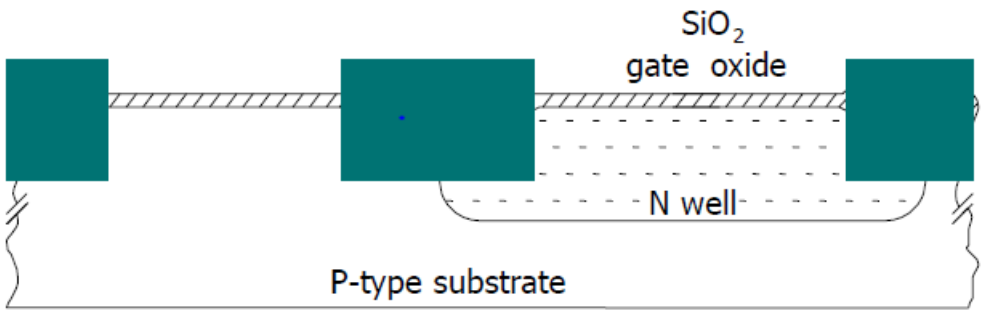


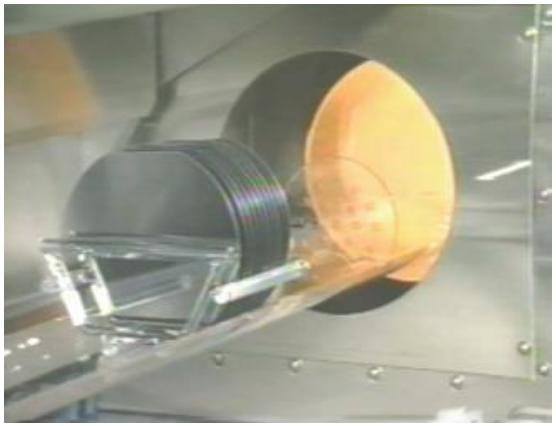
Basic Processing Steps

- Processing is performed on the sliced wafers.
- The wafer is divided to many dies.
- Processing is done in parallel for all dies.
- Two parts:
  - Transfer an image of the desired layer pattern (mask) to the wafer – Photolithography
  - Using that image as a guide, create the desired layer on silicon
    - diffusion (add impurities to the silicon)
    - oxide (create an insulating layer)
    - metal (create a wire layer)



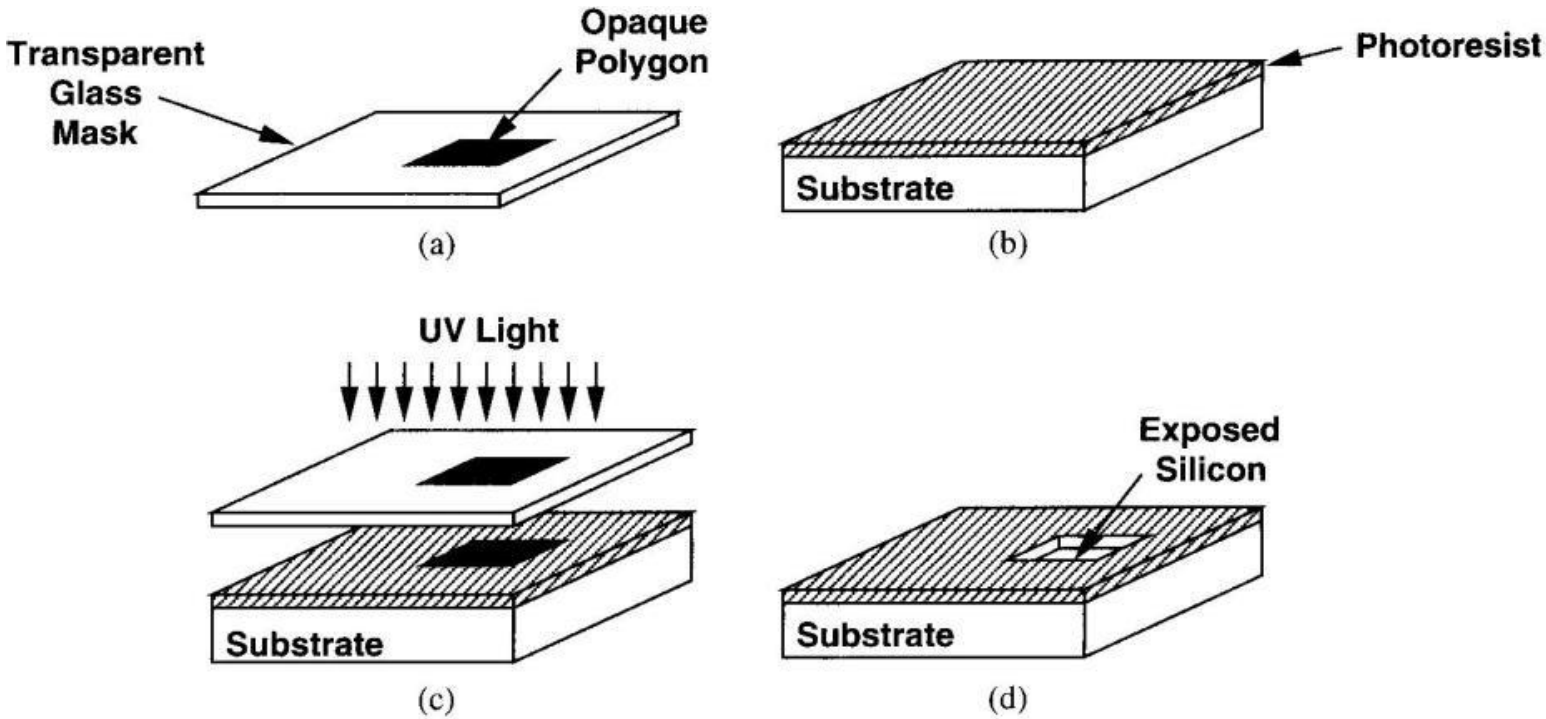
Oxidation





- Si produce a very uniform oxide layer on the surface (few 10s of A°).
- Protective coating in many fabrication steps.
- Grown by placing Si in oxygen at 1000°C.
- Gate oxide:
  - Threshold (current, matching, reliability, …)
  - Cleanness (mobility, current, transconductance, noise, …)

Photolithography



- Negative PR: hardens in the areas exposed to light
- ·Positive PR: hardens in the area NOT exposed to light

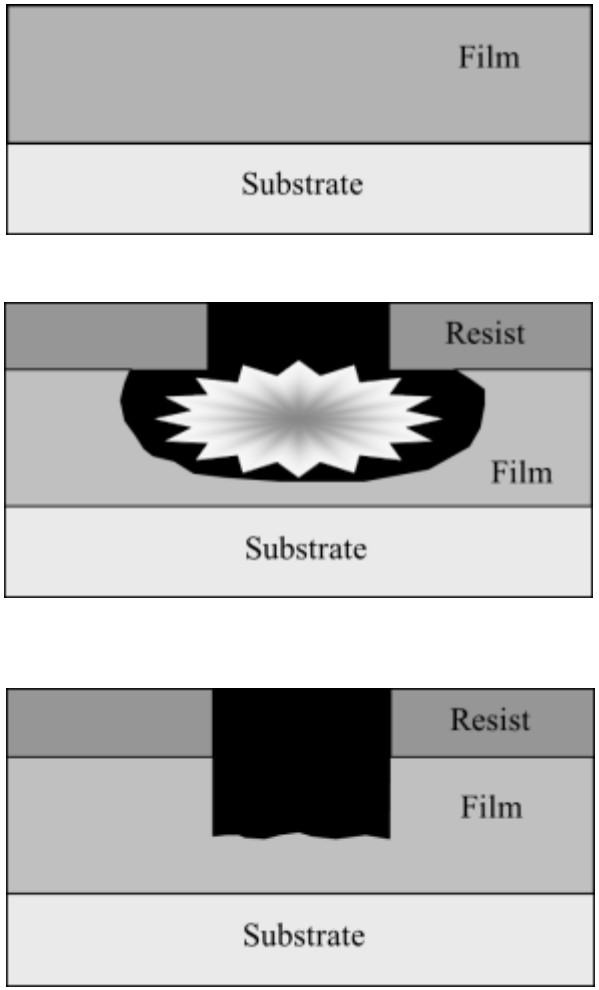
Deposition & Etching

Deposition: material deposition over the complete wafer.

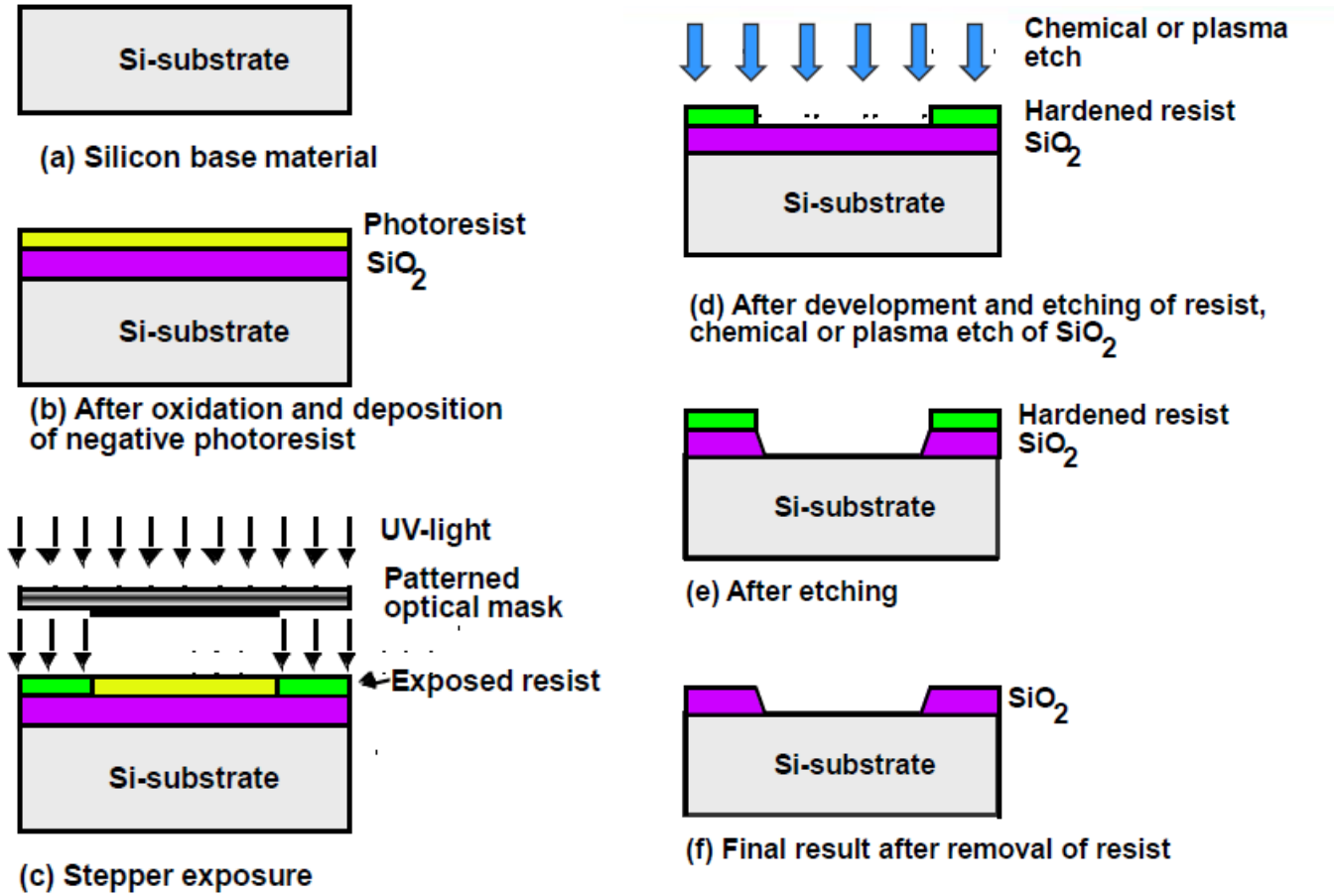
- Chemical Vapor Deposition (CVD): gas reaction under high temperatures.

Etching: selective etching from pre-defined parts on the wafer.

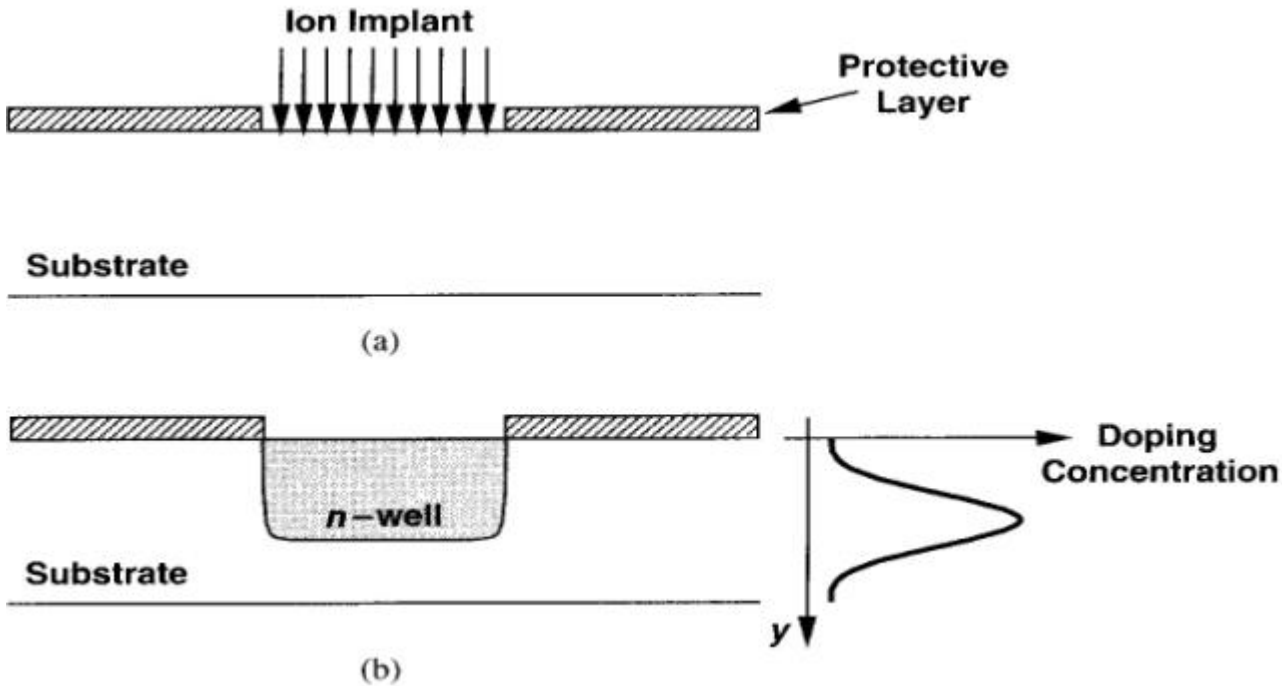
- Wet etching: based on immersing the wafer in acids. Etch in all directions.
- Dry (plasma), Reactive Ion Etching (DRIE): uses +ve heated ions to etch a –vely charged wafer in a vacuum chamber. Vertical etching.



Patterning of SiO2 – Windows for Processing



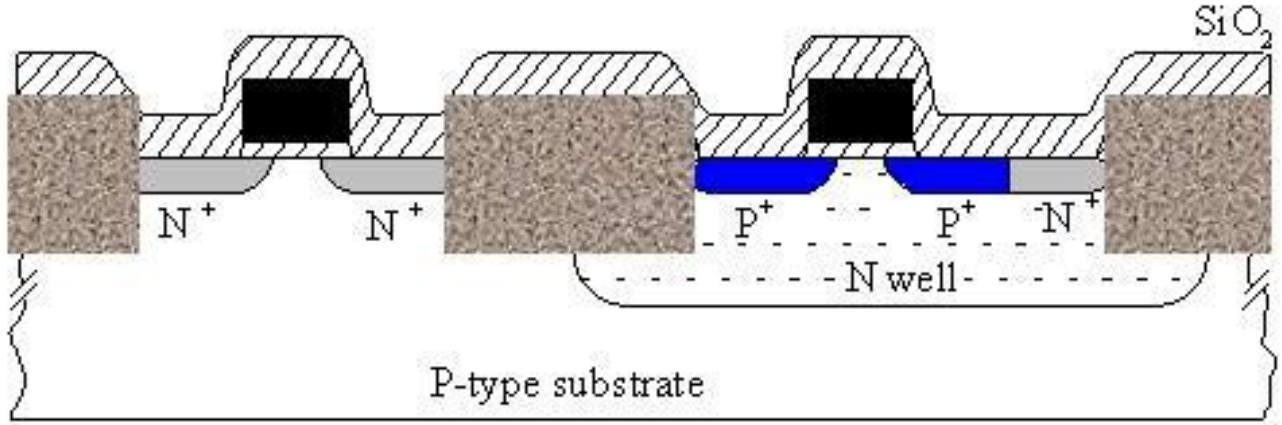
Ion Implantation



- Doping atoms are accelerated, focused to hit the surface.
- Damages the lattice.
- Followed by annealing (heating to 1000°C for 15-30 min.)
  - Lattice bonds are repaired
  - Diffusion of dopants.

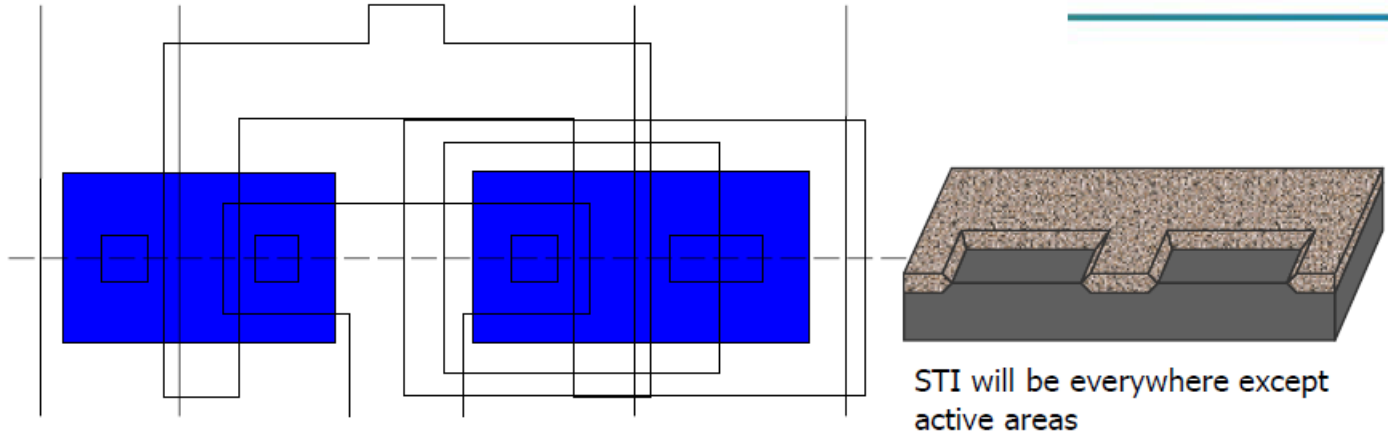
Chemical Mechanical Polishing (CMP)

- In modern CMOS processes, multiple metal interconnect layers are superimposed onto each other.
- During lithography, topography variation in the thin film over which the photoresist is spun causes pattern lens defocusing.
- The wafer surface must be flat.

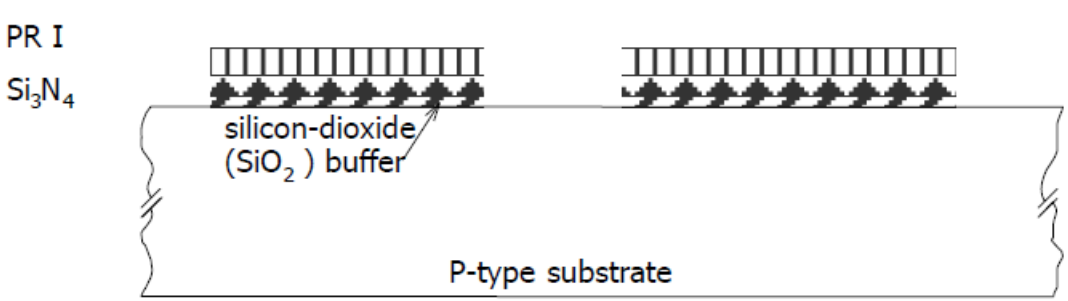


Process Flow: CMOS Inverter

Shallow Trench Isolation – Definition

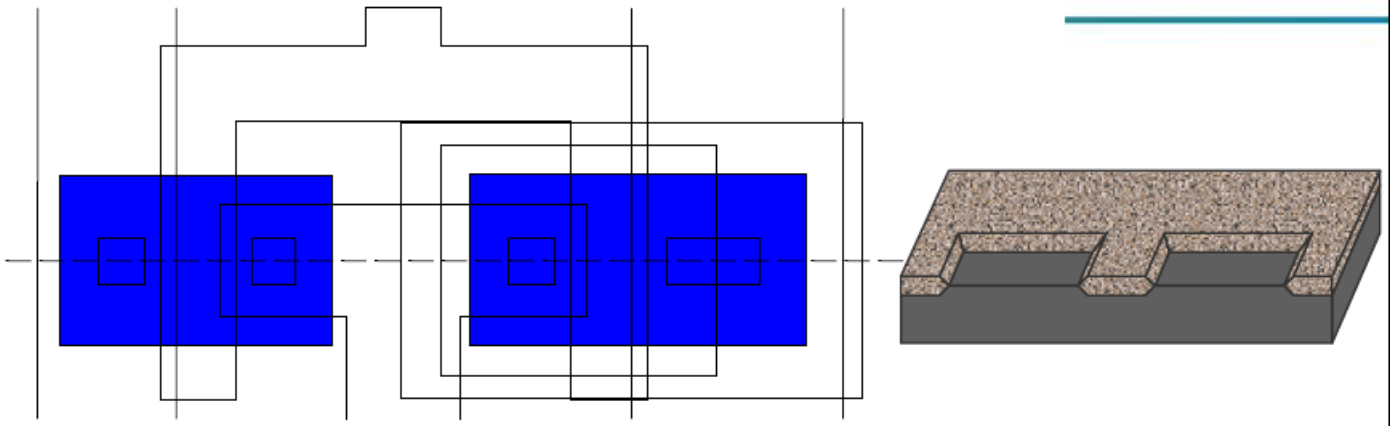


(a)



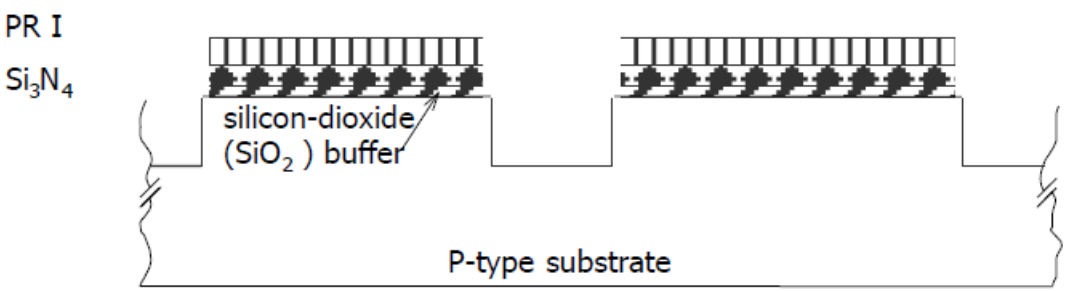
- thermal oxidation (buffer SiO_2)
- chem.-vapor deposition (CVD) of Si_3N_4
- Photolithography I (+ve): definition of active areas (transistor areas)

STI Etching

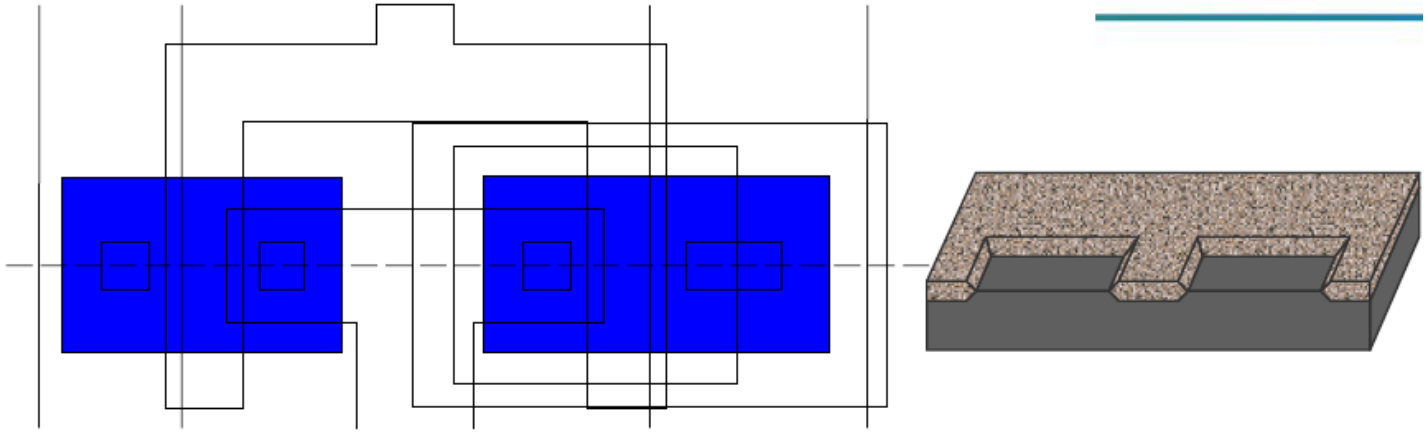


(b)

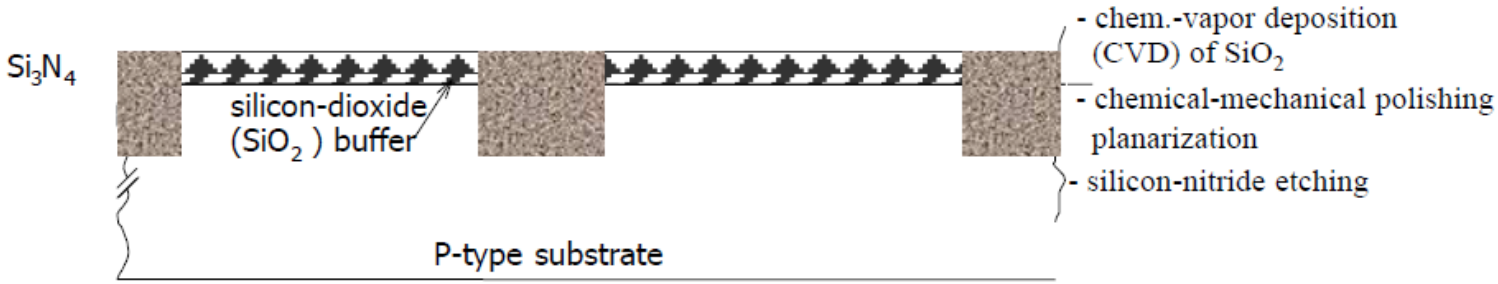
- Reactive Ion Etching (RIE)



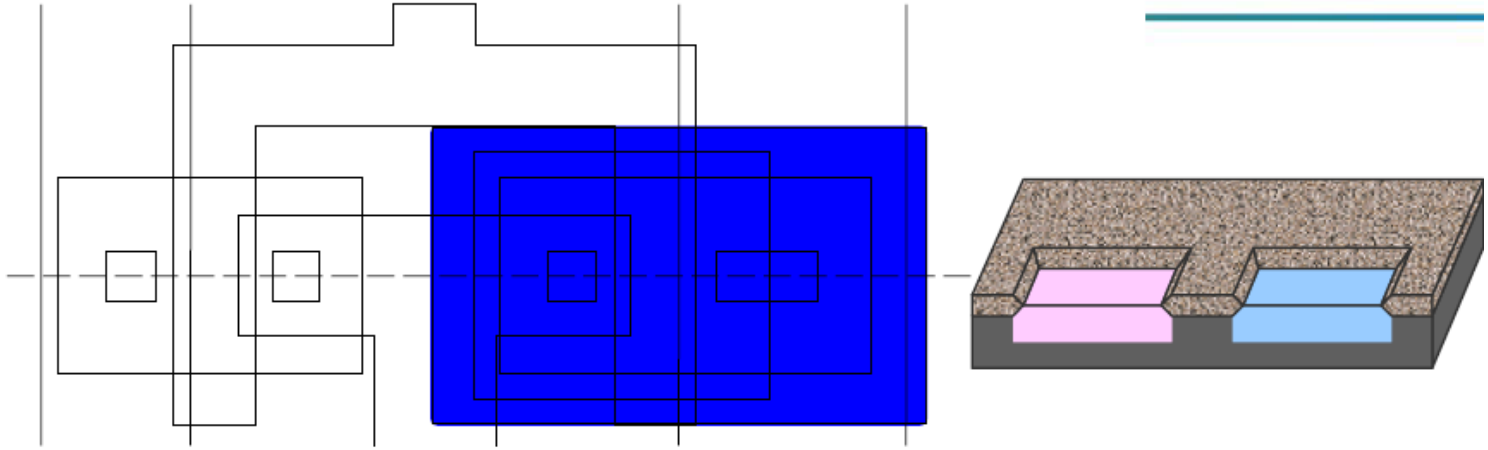
STI Fill

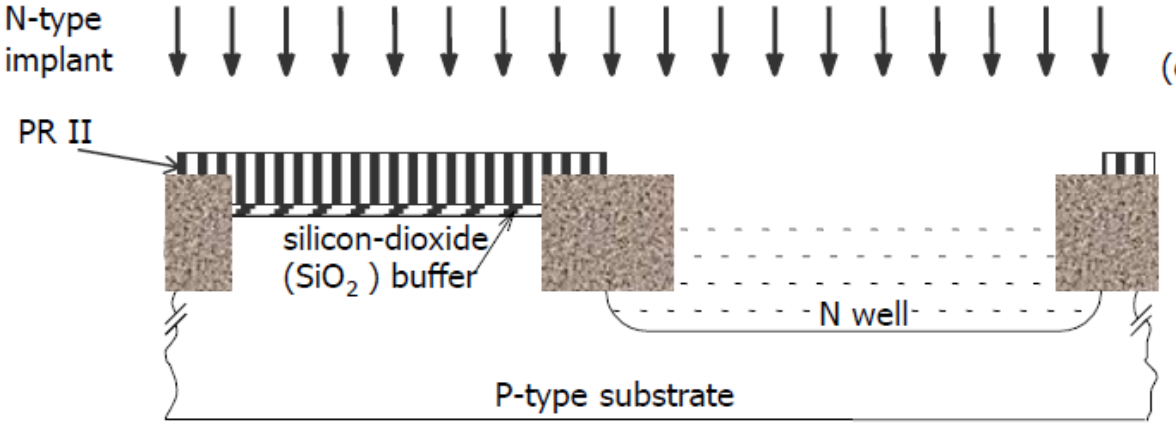


(c)

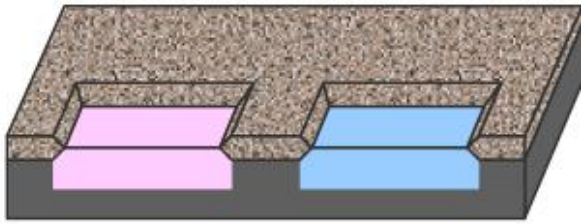

Si_3N_4
silicon-dioxide
(SiO_2) buffer
P-type substrate
- chem.-vapor deposition (CVD) of SiO_2
- chemical-mechanical polishing planarization
- silicon-nitride etching

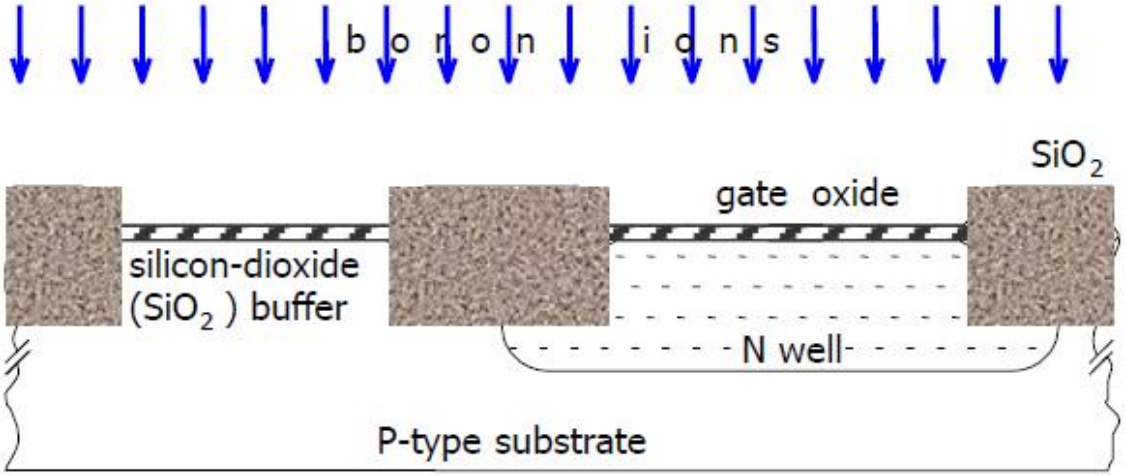
Well Implant





- Photolithography II: N-well implant windows
- N-well implant and drive-in
- oxide etching
- optional P-well

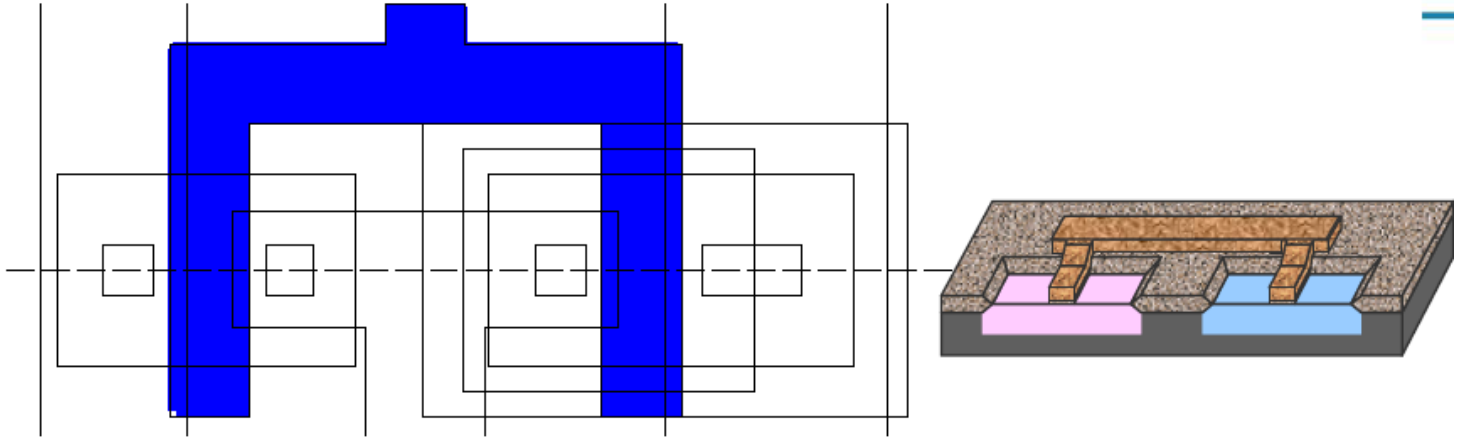




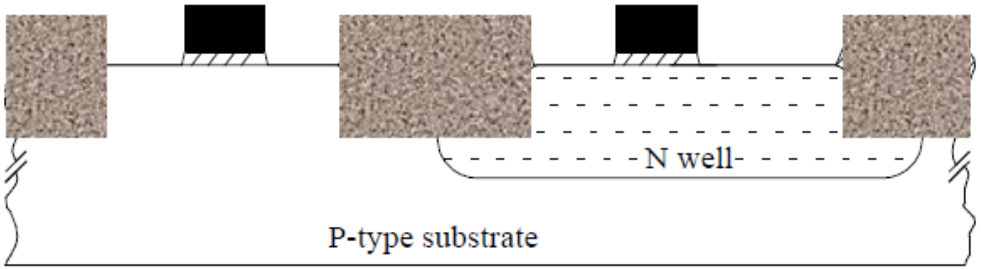
(e)

- buffer oxide etching
- surface cleaning
- gate oxide growth
- threshold-voltage adjustment implant.
- adjustment can be done per transistor type using the well mask or for both simultaneously

Gate Patterning

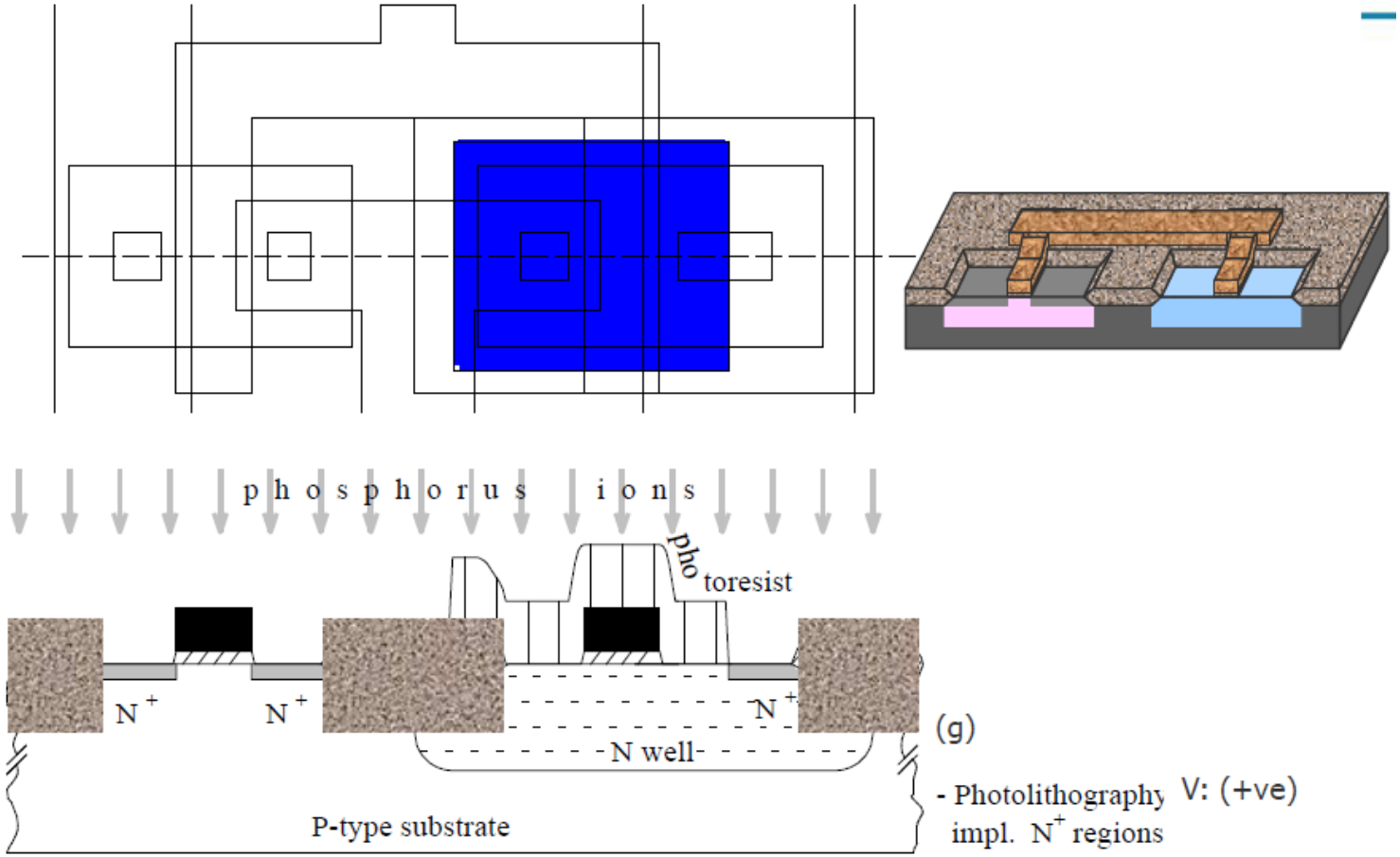


(f)

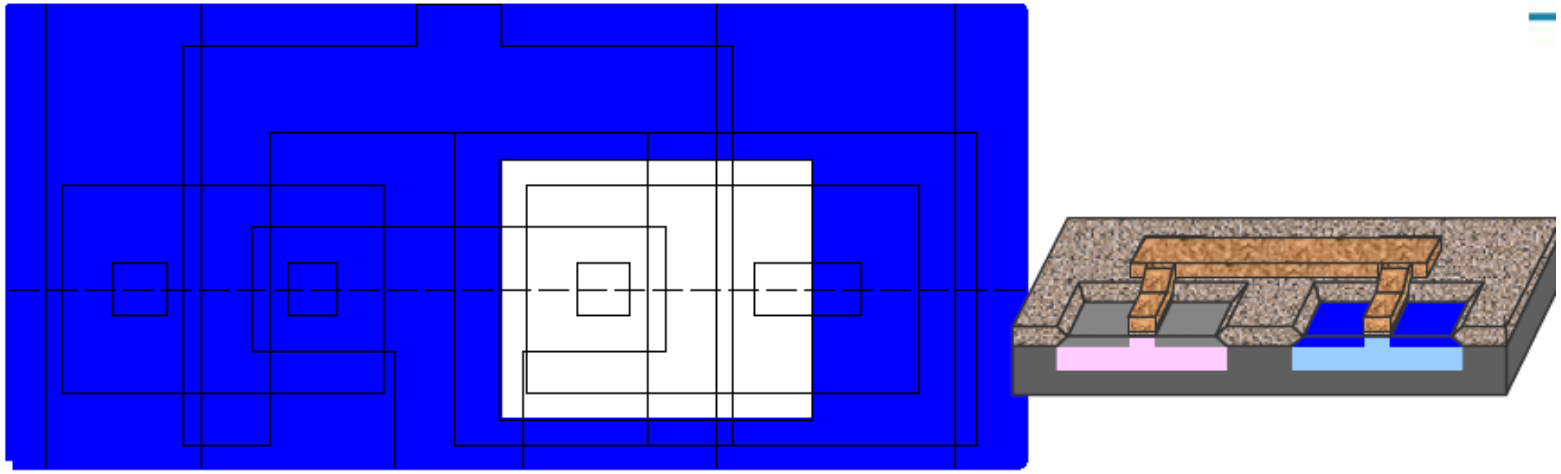


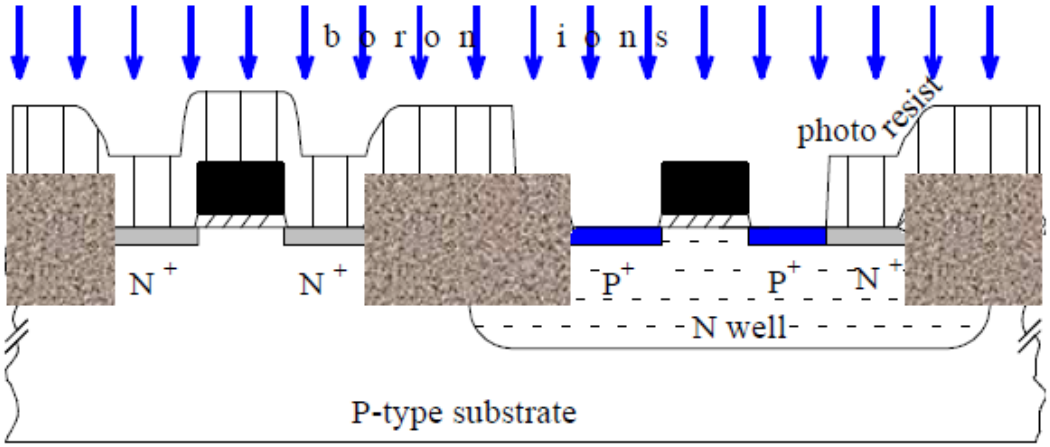
- Chem.-vapor deposition (CVD) of N^+-doped polysilicon
- Photolithography IV: (+ve) polysilicon patterning (gate definition)
- gate-oxide etching

N+ Implant (Select)



P^+ Implant (Select)

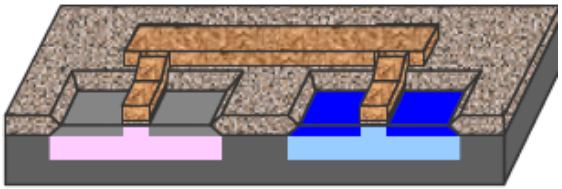


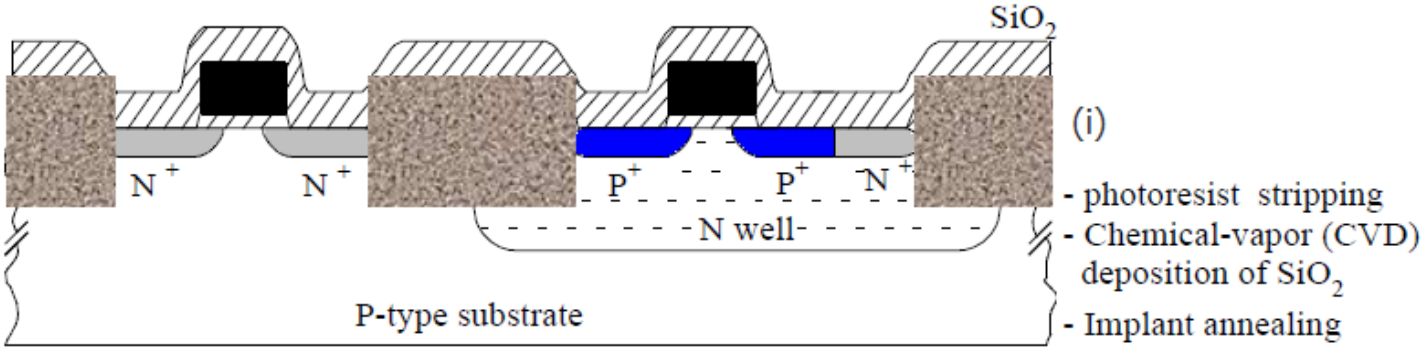


(h)

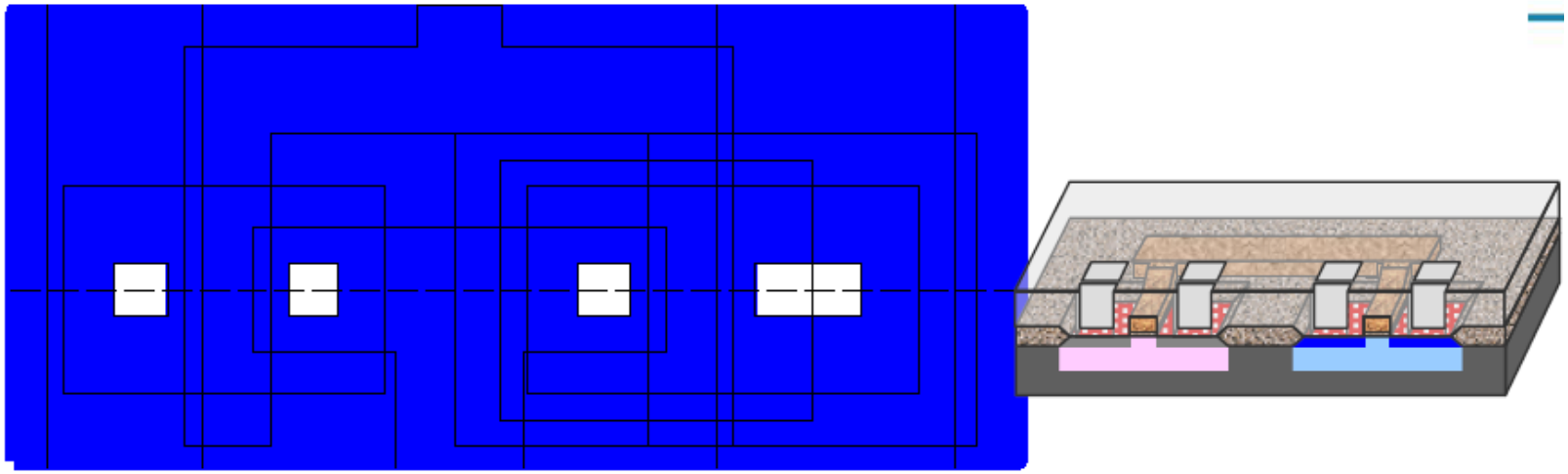
- photoresist stripping
- Photolithography VI: (–ve)
impl. P^+ regions

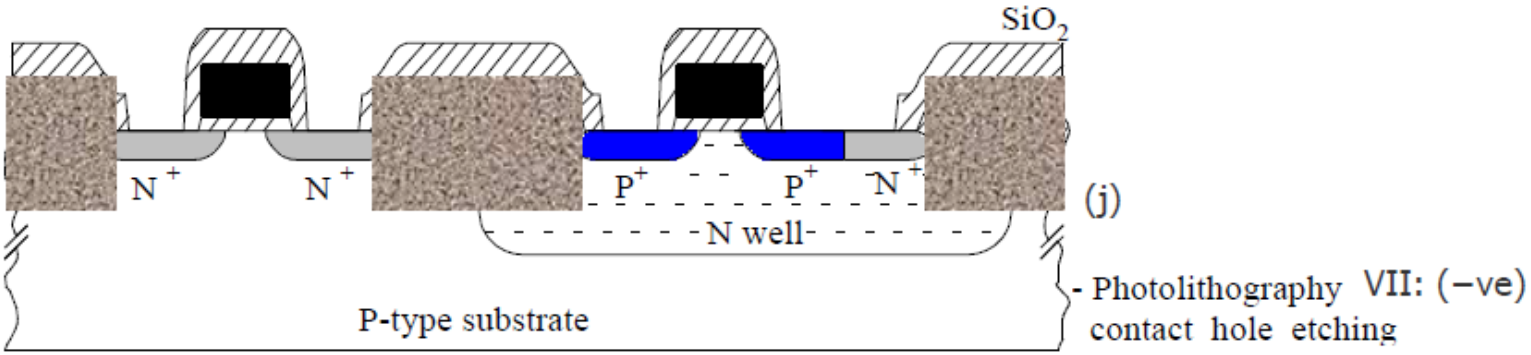
Implant Annealing



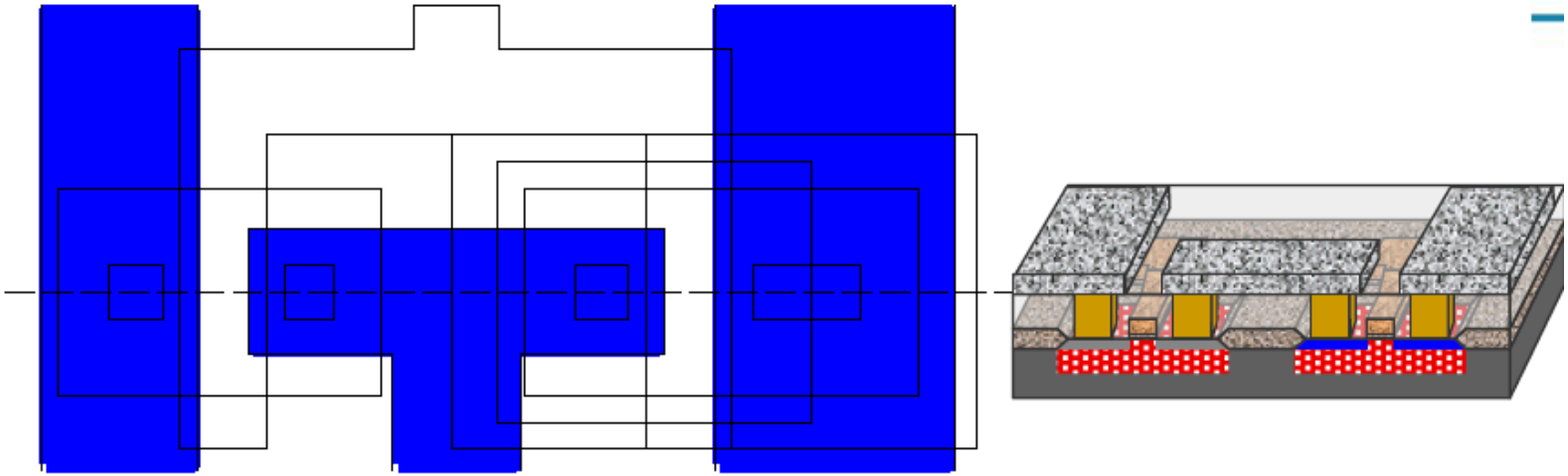


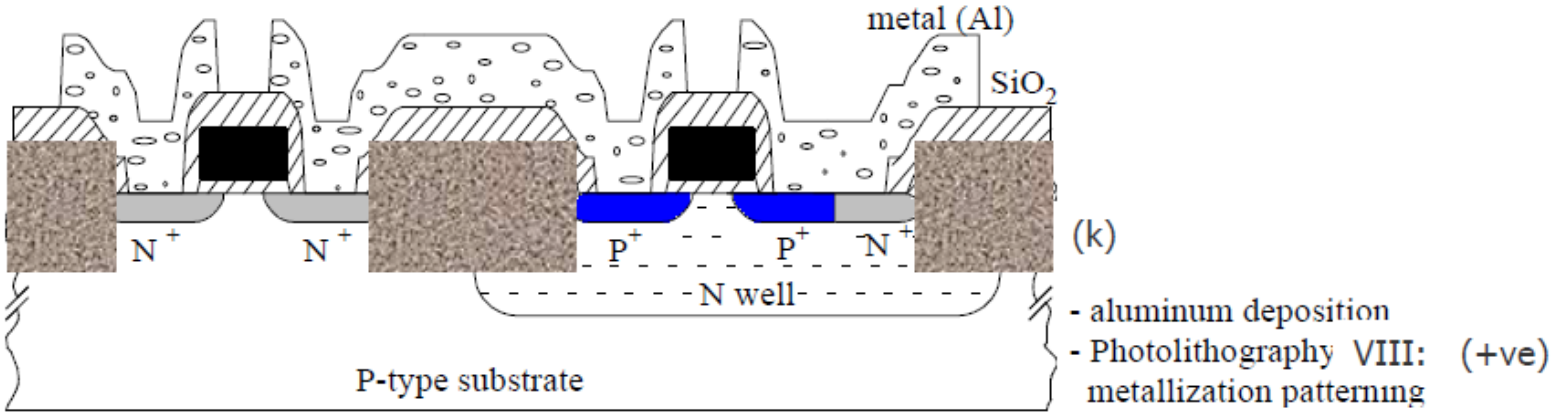
Contacts




SiO2
N+
N+
P+
P+
N+
(j)
N well
P-type substrate
- Photolithography VII: (−ve)
contact hole etching

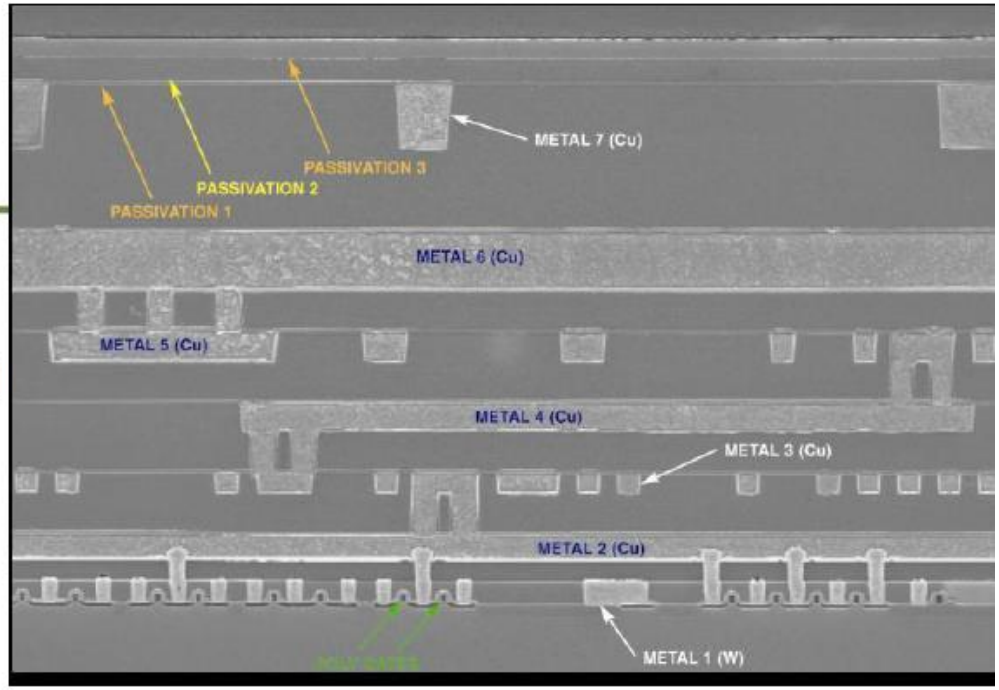
Metal 1 Patterning

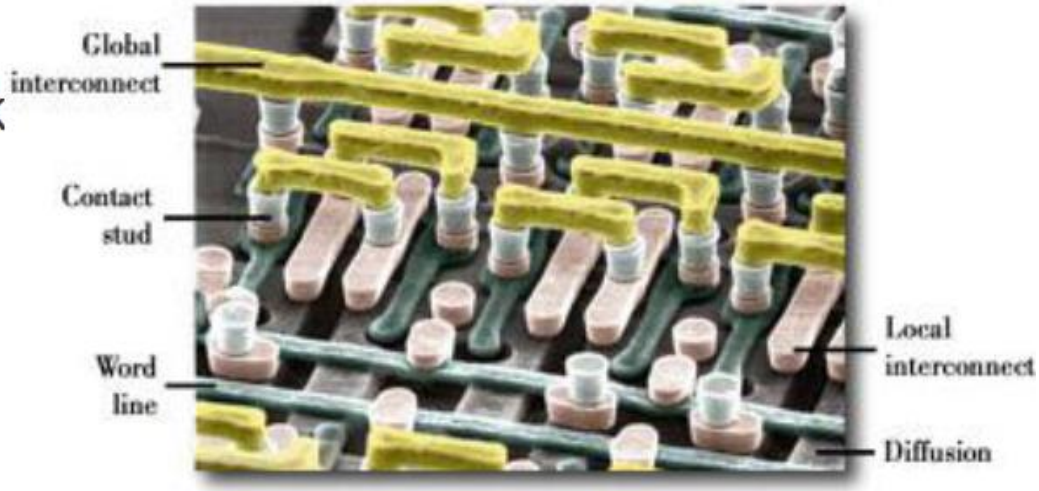




Metalization

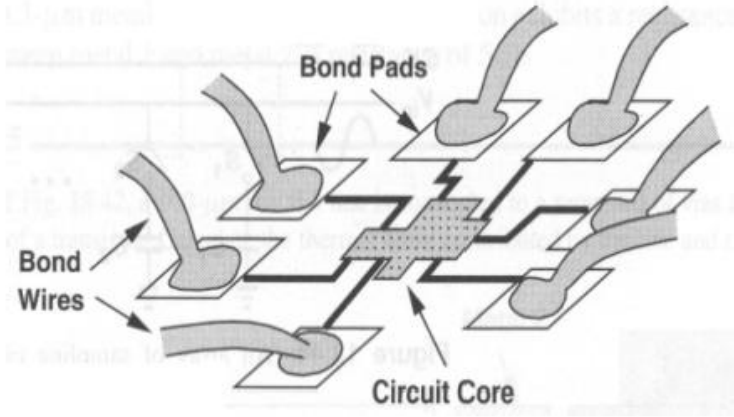
- The same contact opening – metalization processes is repeated for several layers of metal.
- For each additional metal layer two mask are required:
  - — contact windows
  - — metal itself.





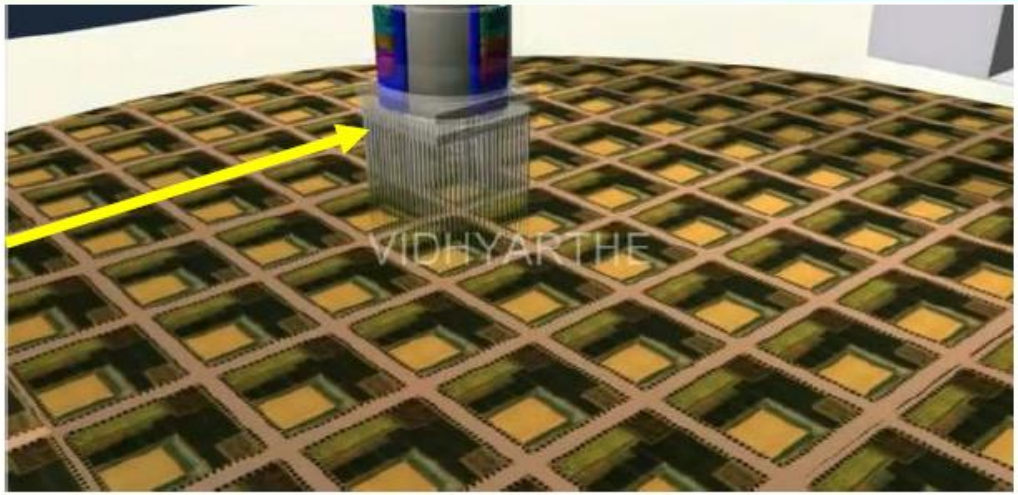
Passivation

- The final step is to cover the wafer with a glass (passivation) layer, protecting the surface against subsequent mechanical handling and dicing.
- The passivation mask is used to open the glass only on top of the bond pads to allow external connection (packaging).



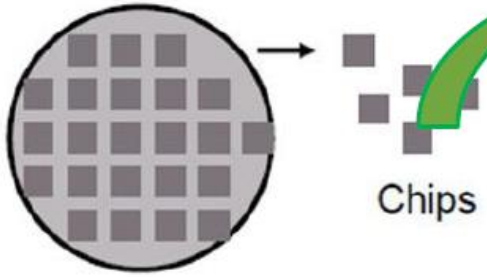
On-Wafer Test

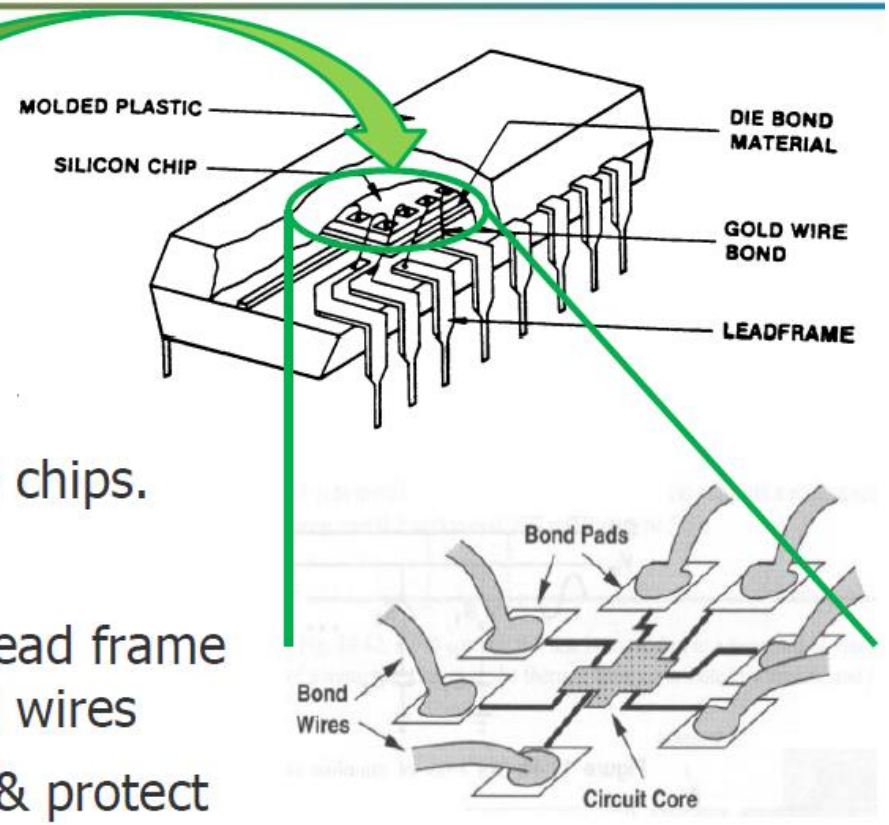
Probe card



- Each die is tested separately for functional defects by applying special test patterns.
- For electrical testing a set of microscopic contacts called a *probe card* aligned with chip input/outputs are used.
- Faulty chips are marked and later discarded.

Packaging





- Wafer sliced to multiple chips.
- Each is packaged
- I/Os connected to the lead frame using aluminum or gold wires
- Packages remove heat & protect the die against environment.

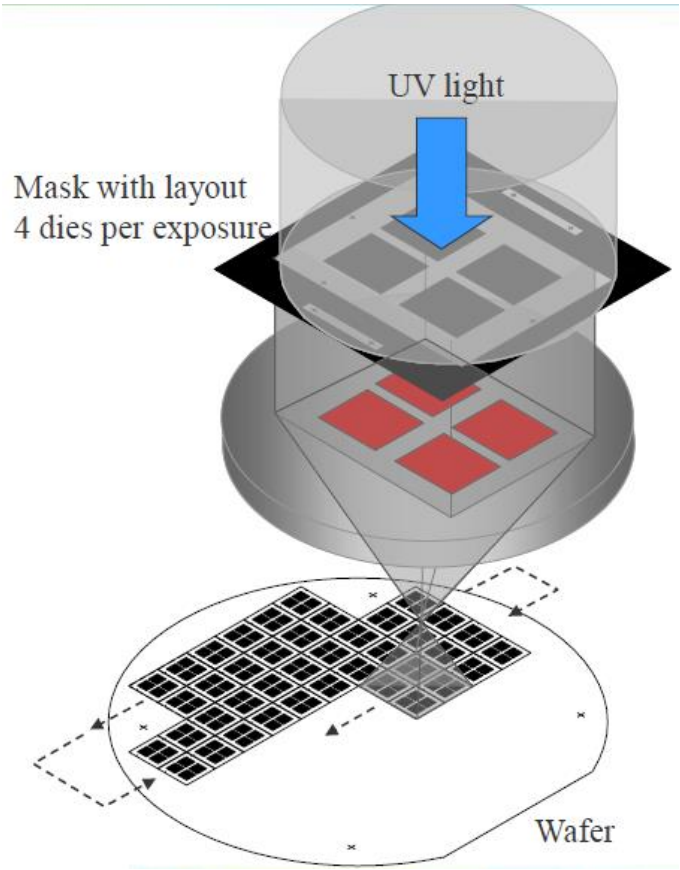
Advanced Process Developments

- OPC
- Double Patterning
- FinFETs

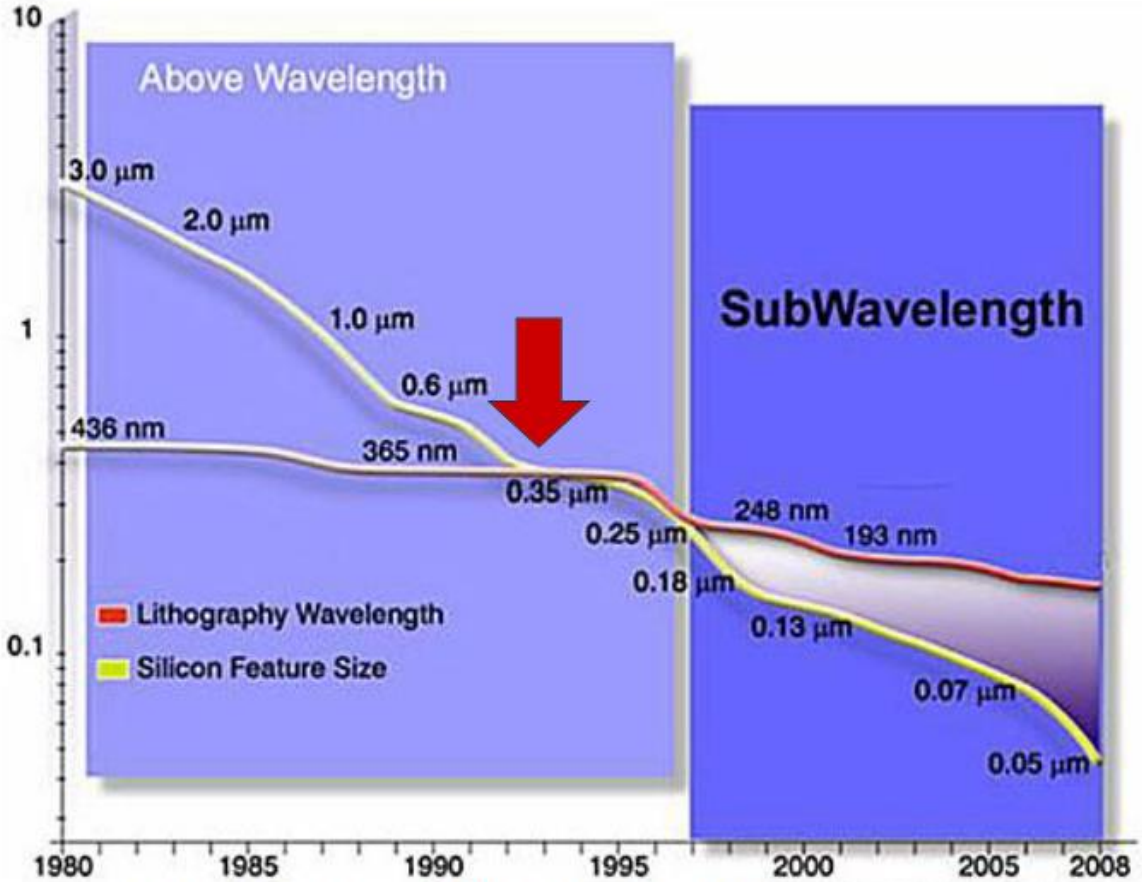
Limits of Optical Lithography

Transistor dimensions keep scaling down while the wavelength of the UV light source is not.

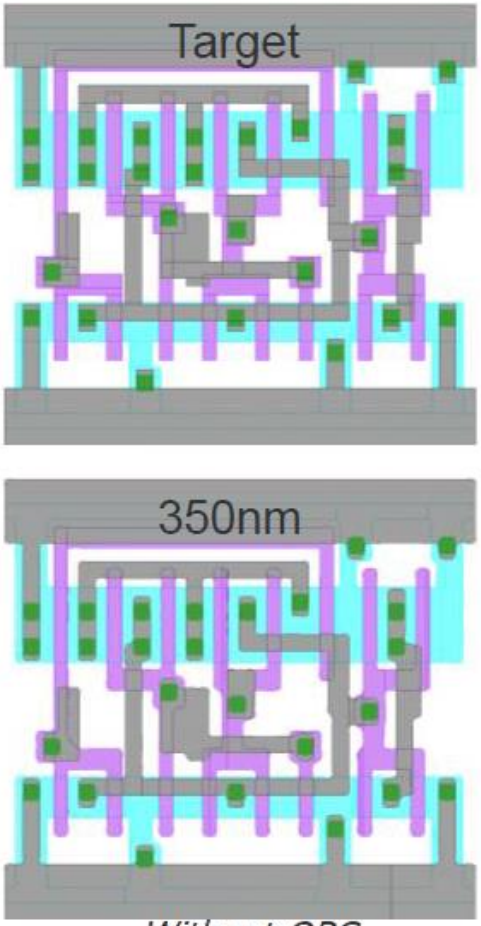
Can’t define shapes less than the wavelength!!



Optical Proximity Correction – OPC

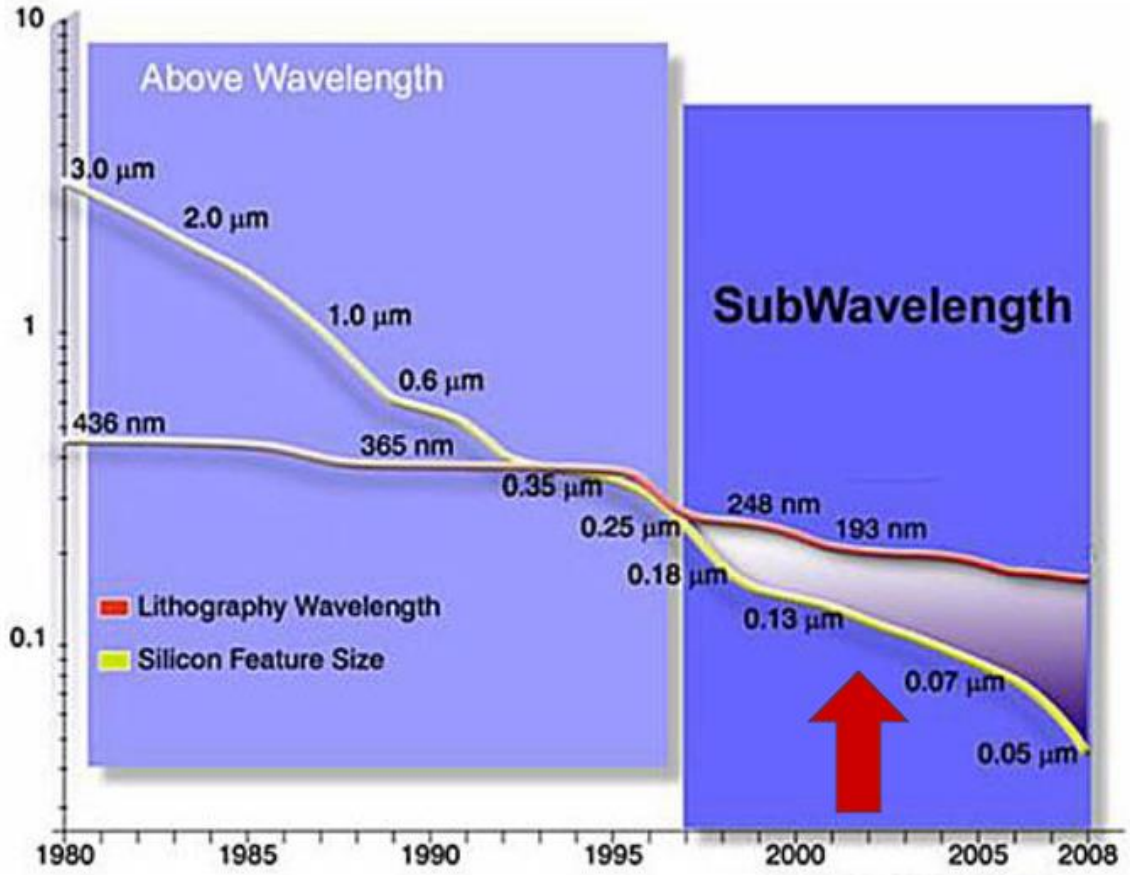


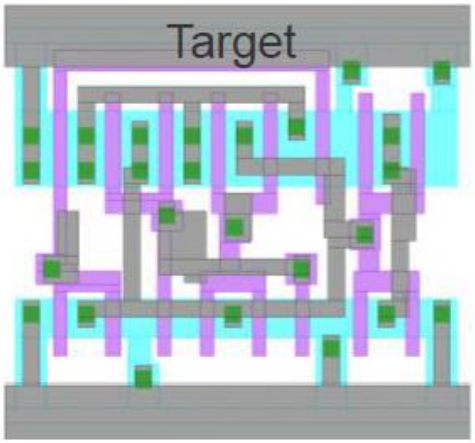
A micron is one-millionth of a Meter
Diameter of a human hair is 100µm

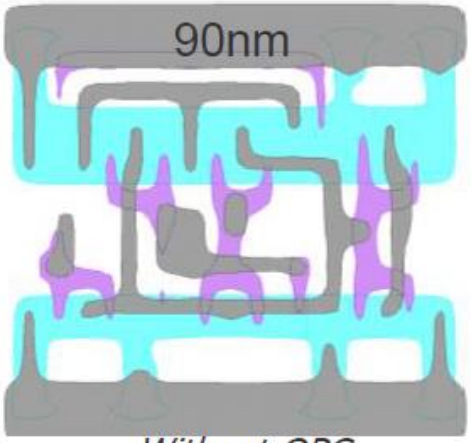


Without OPC

Optical Proximity Correction – OPC



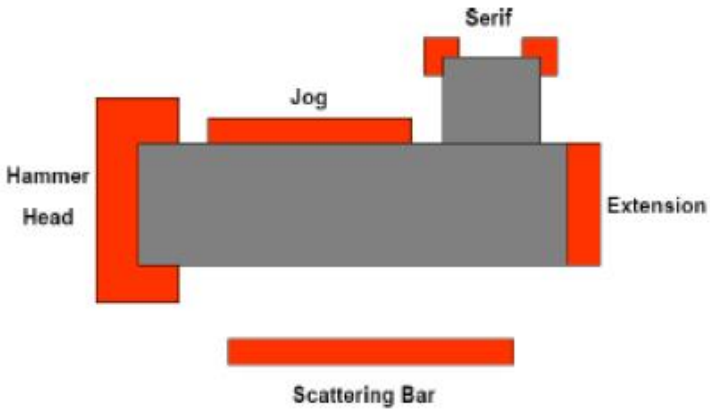


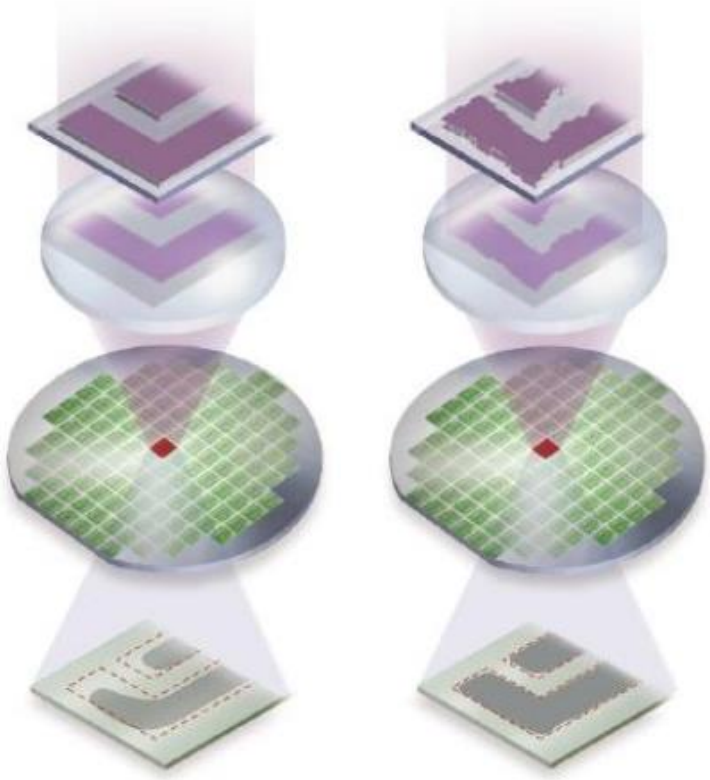


Without OPC

Optical Proximity Correction – OPC

- OPC: Increase the number of diffraction orders of light by slightly changing the pattern.
- Tool: Calibre OPC



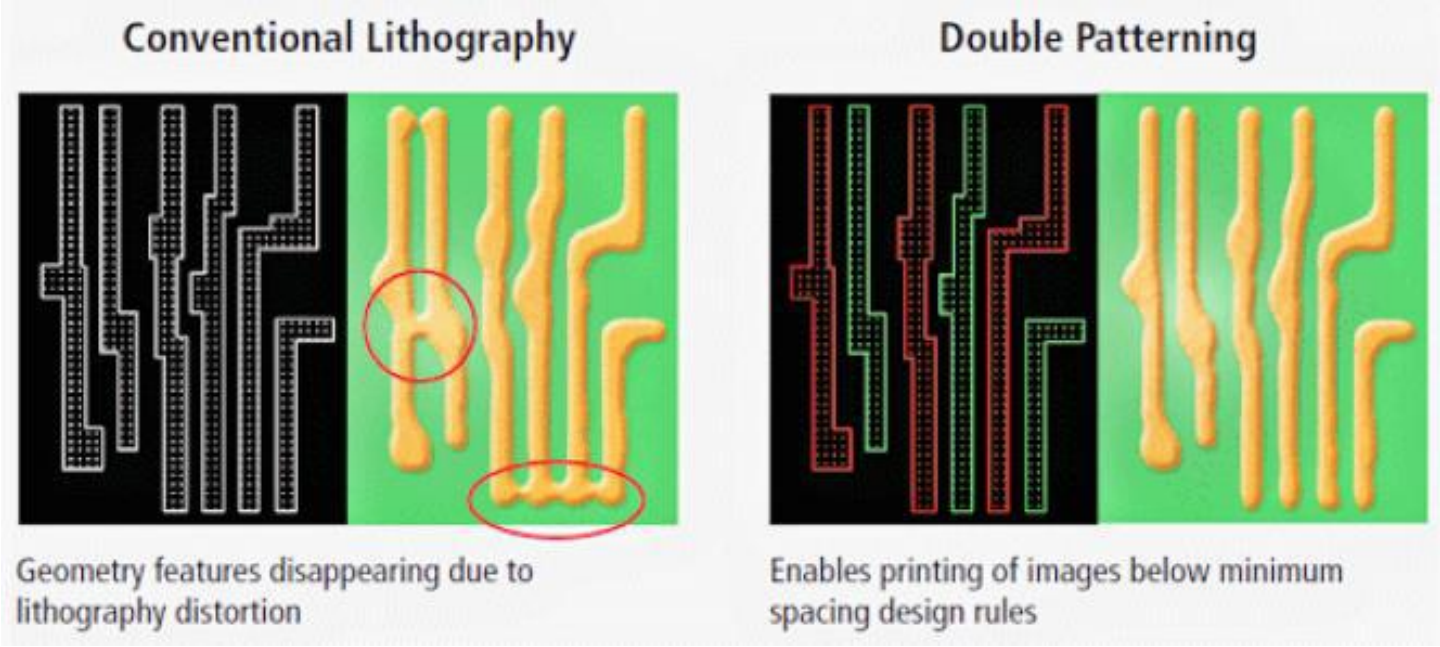


OPC: Designer viewpoint

- This is a back-end flow, done after tape-out
- Designers are unaware of OPC for the most part
- Only real restriction: limit use of 45o routing
  - 45° routes, with OPC, need more spacing to other wires
- OPC does explode the database size
  - Imagine the size of a microprocessor database...

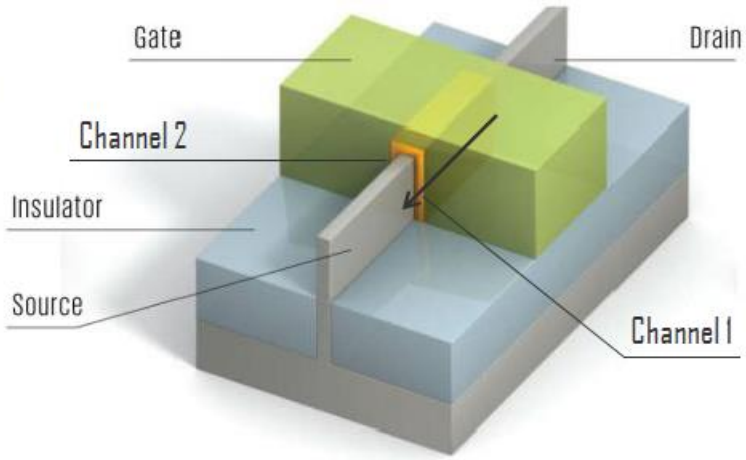
Below 28 nm: Double Patterning

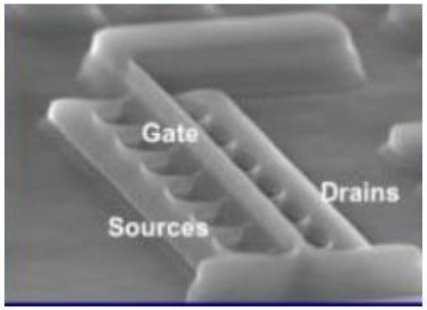
- Close lines are shorted due to light diffraction.
- Concept: Split pitch into two masks -> Double pitch density.



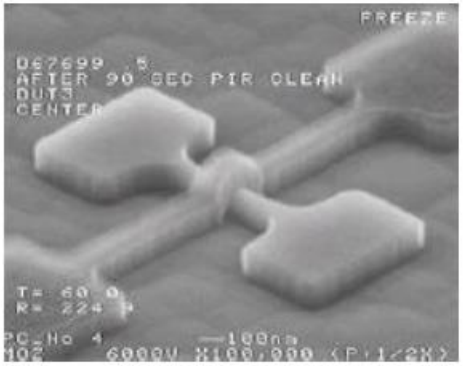
FinFET

- Solution: Add another gate
- FinFET: Double gate MOSFET
- Fabricated on top of the substrate.
- Compatible with CMOS processing technology.
- Already in production at Intel 22 nm process.
- Discrete W





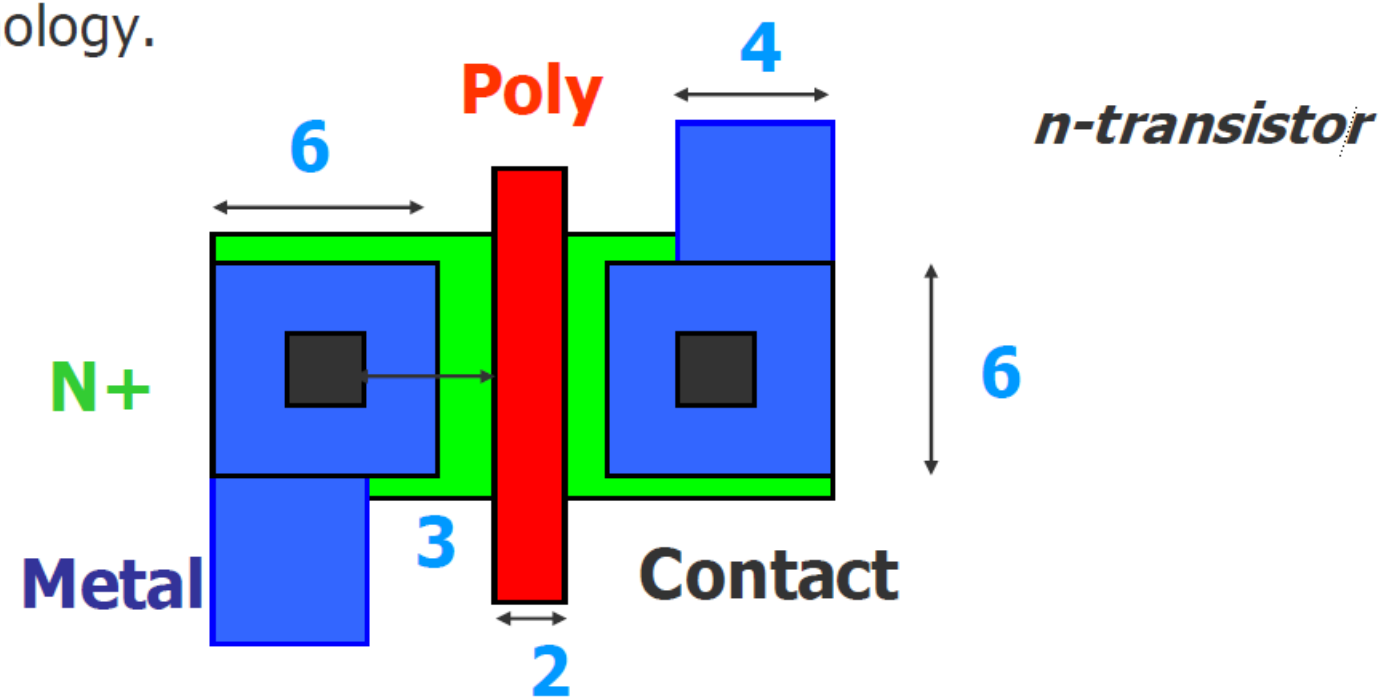
Multi-fin device



- Layout Basics
- Design Rules
- Design Rule Evolution

Layout Layers

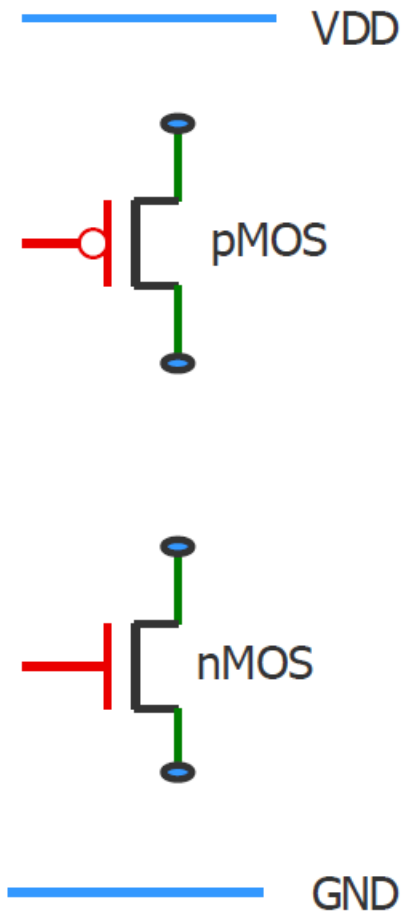
- It consists of a pattern of rectangular color-coded areas.
- Different colors ("layers") correspond to different physical regions or layers available in the target fabrication technology.

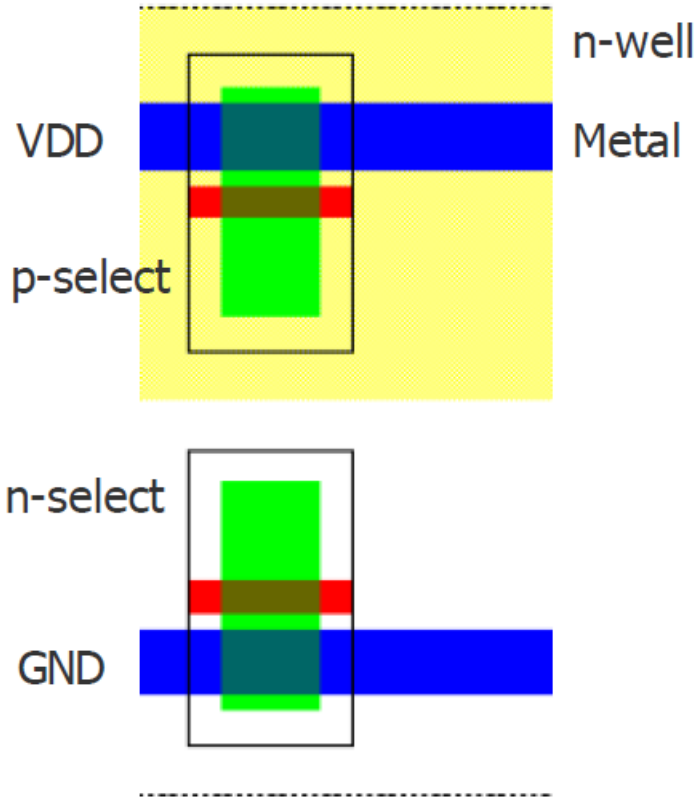


Example: CMOS Process Layers

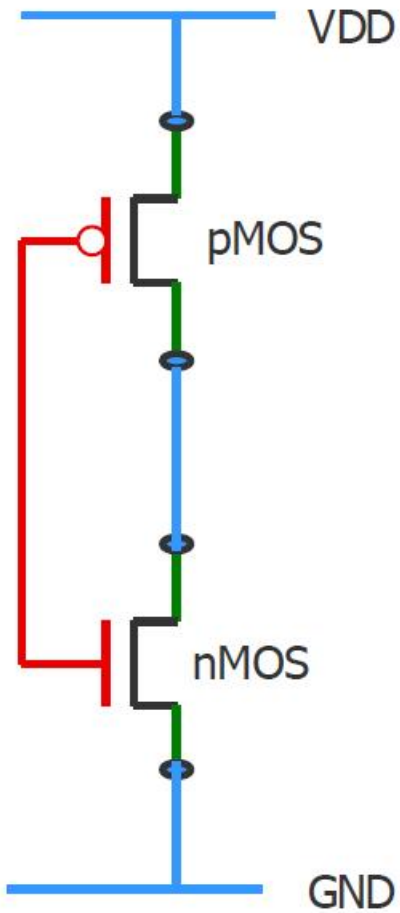
Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

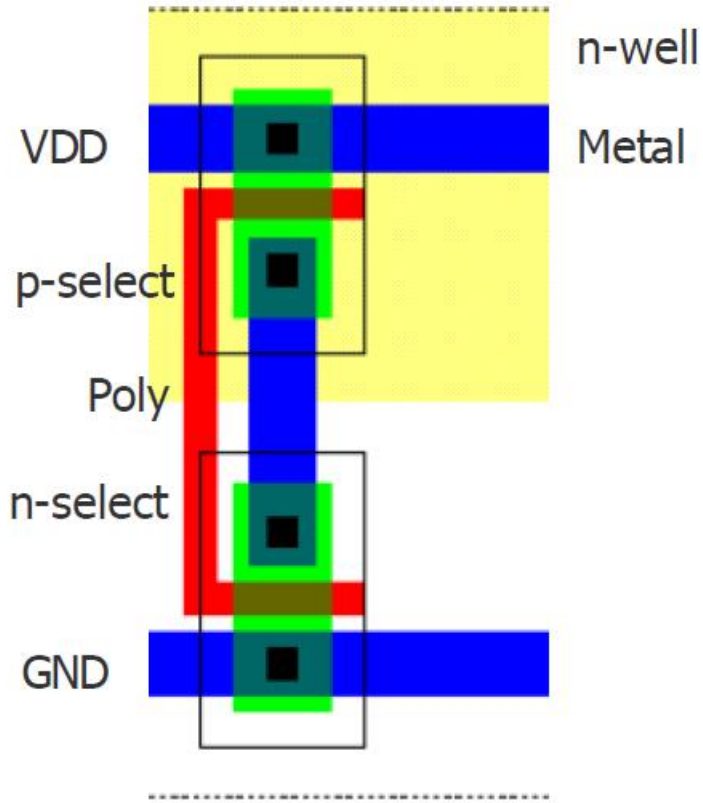
CMOS Inverter Layout: Transistors



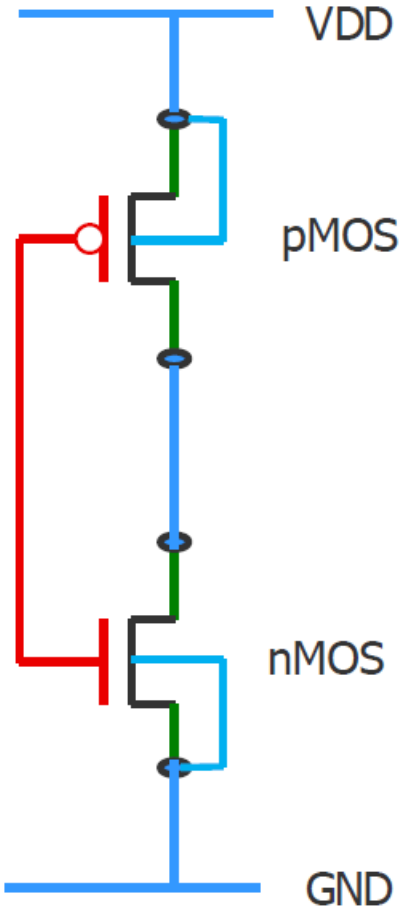


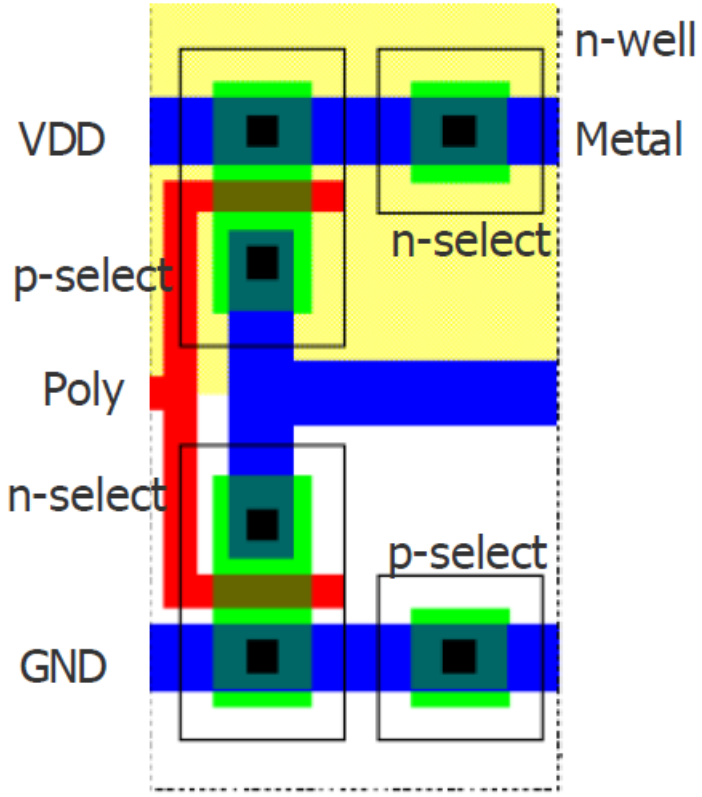
CMOS Inverter Layout: Routing





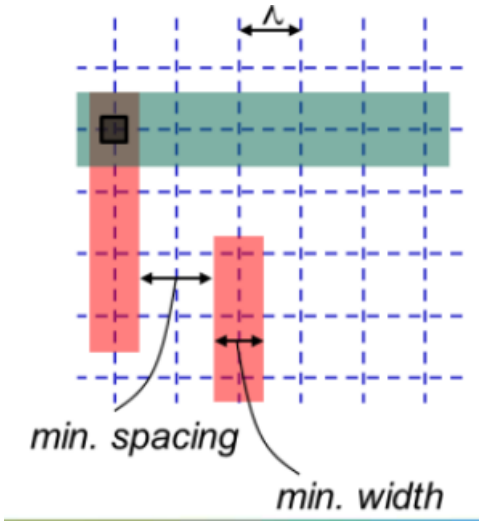
CMOS Inverter Layout: Bulk Contacts





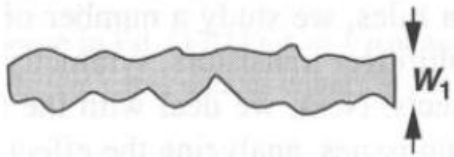
Design Rules (DR)

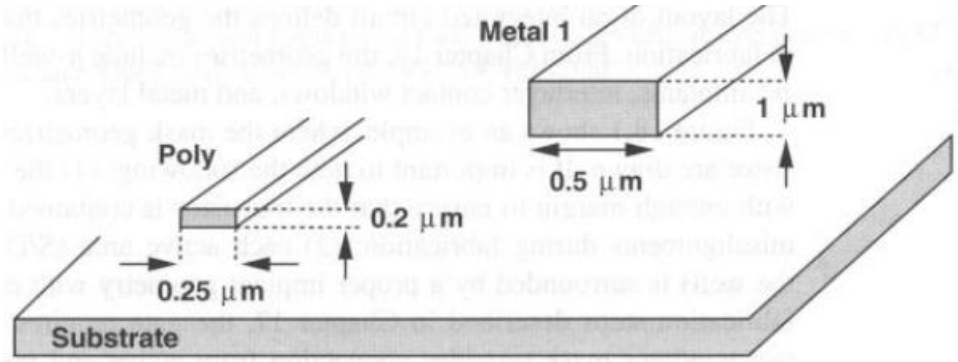
- A set of rules that guarantees proper fabrication despite various tolerances in each step of processing.
- Designer determines transistor W & L, DR dictate the rest.
- Interface between designer and foundry.
- Guidelines for constructing process masks.
- Dimensions:
  - scalable design rules: (good old days!!)
    - All dimensions in integer multiples of ·
    - Eases technology changes with minimum cost
    - Not optimum
  - absolute dimensions (micron rules)



Design Rules: Minimum Width

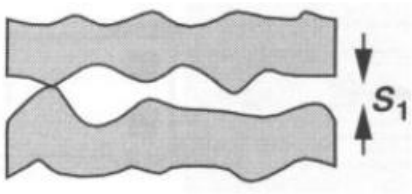
- Geometries must exceed a minimum value imposed by processing capabilities of the technology.
- If a rectangle is excessively narrow, it may break due to tolerances.
- The thicker the layer, the greater its minimum allowble width.

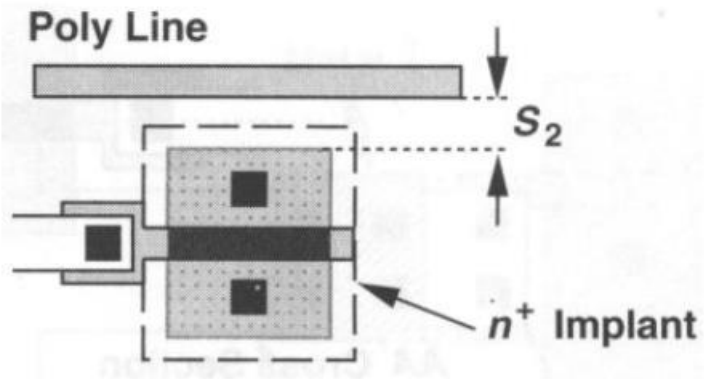




Design Rules: Minimum Spacing

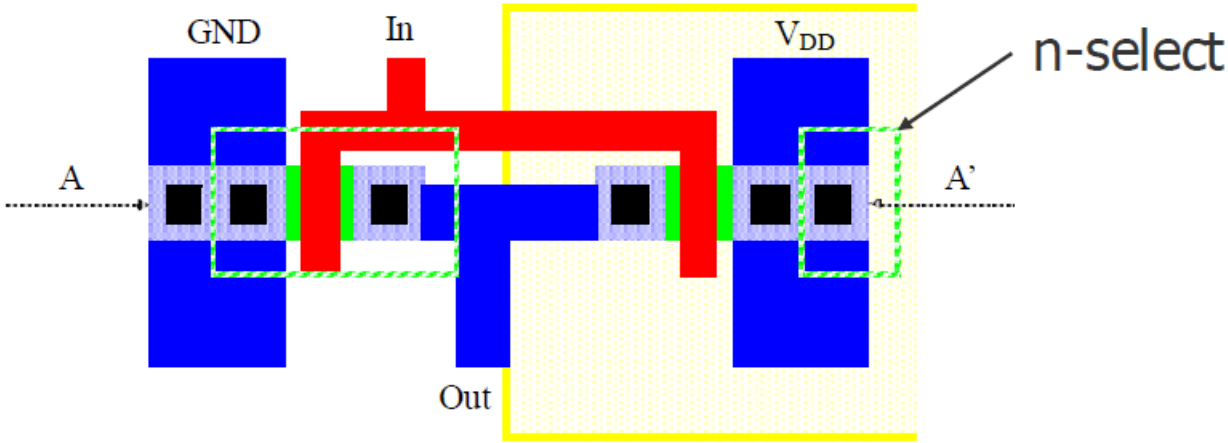
- On the same mask: to avoid that two paths become shorted if placed too close.
- On different masks: to avoid parasitic devices.





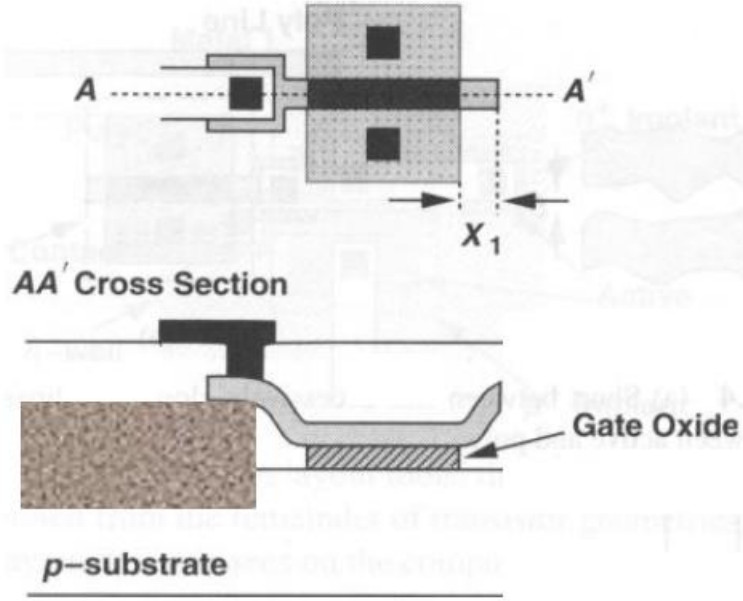
Design Rules: Minimum Enclosure

- Ensures enclosure (geometries completely inside other geometries) despite mask misalignments.
- Transistors surrounded by well and select masks with sufficient margin.
- Contacts surrounded by enough margin of both materials to be contacted.



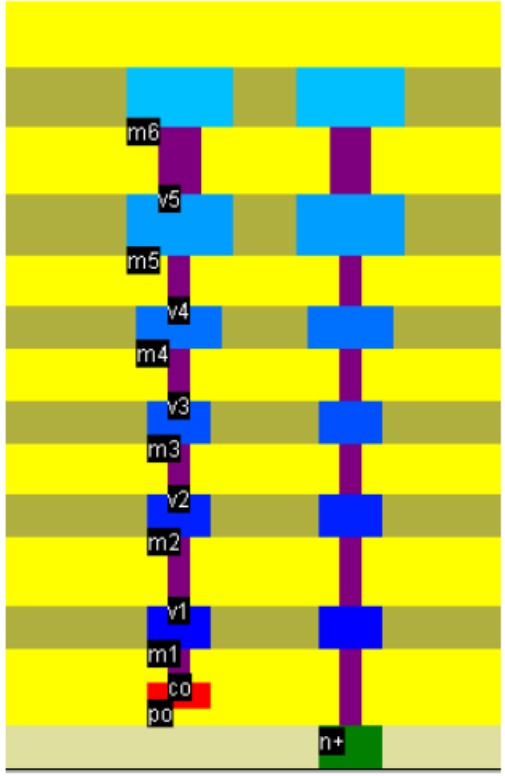
Design Rules: Minimum Extension

- Some geometries must extend beyond the edge of others by a minimum value.
- The gate polysilicon must have a minimum extension beyond the active area to ensure proper transistor action at the edge.



Contacts and Vias

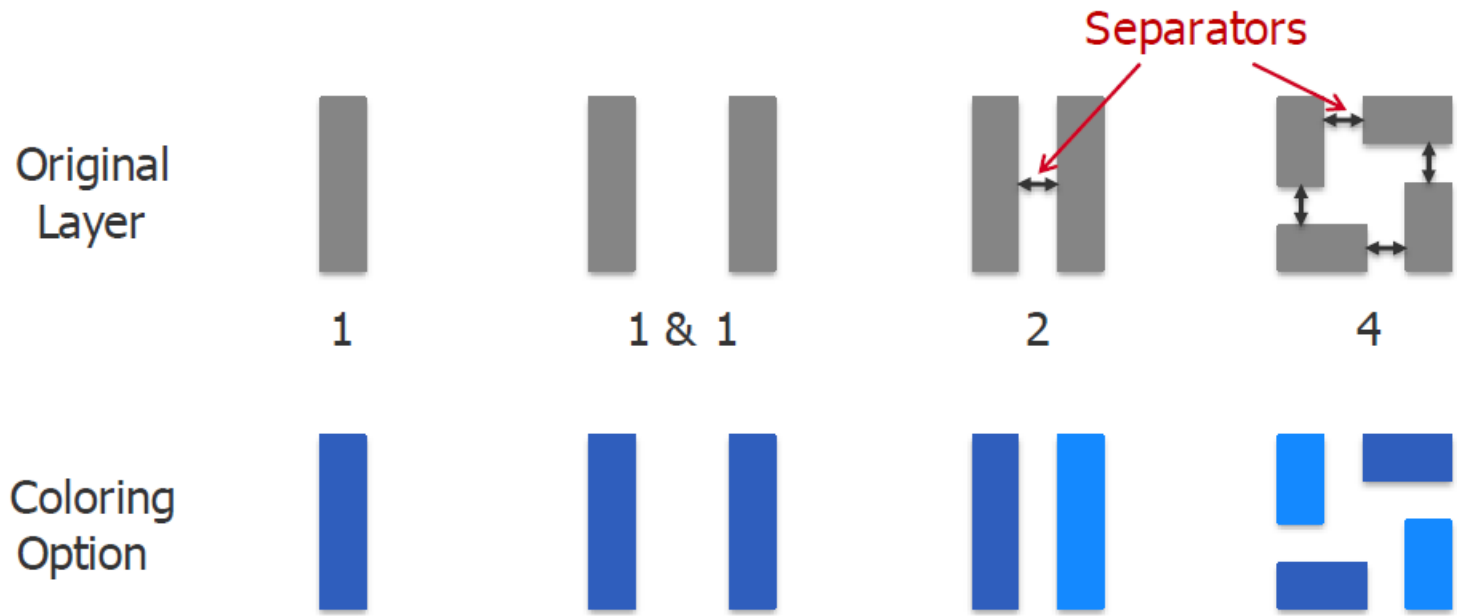
- For example, to contact Metal3 to the poly, the following masks should be used:
- Poly-C-M1-V1-M2-V2-M3
- The higher the metal level, the thicker the metal, and the lower the sheet resistance.



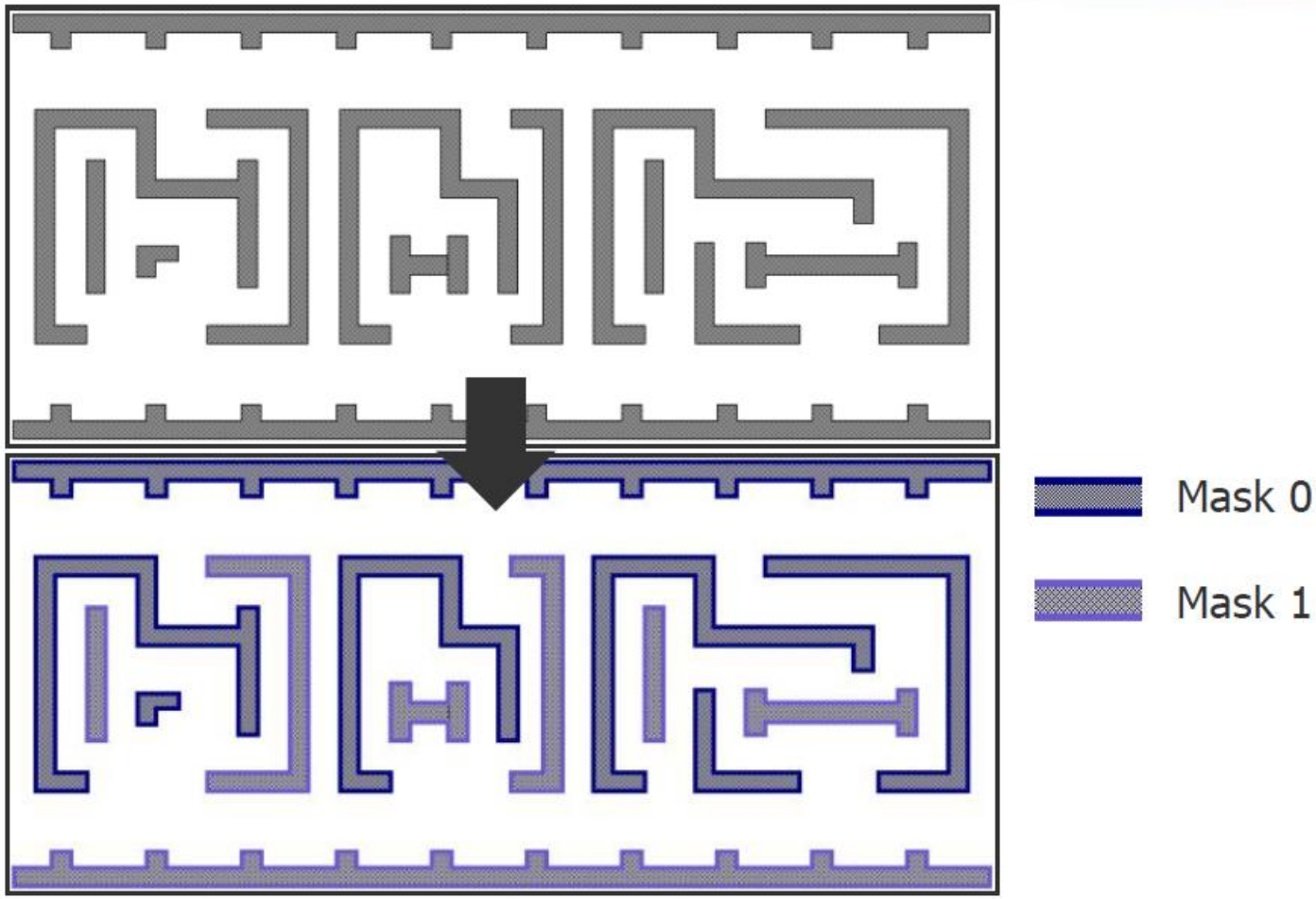
Metal-Via stack

Double Patterning Decomposition (Coloring)

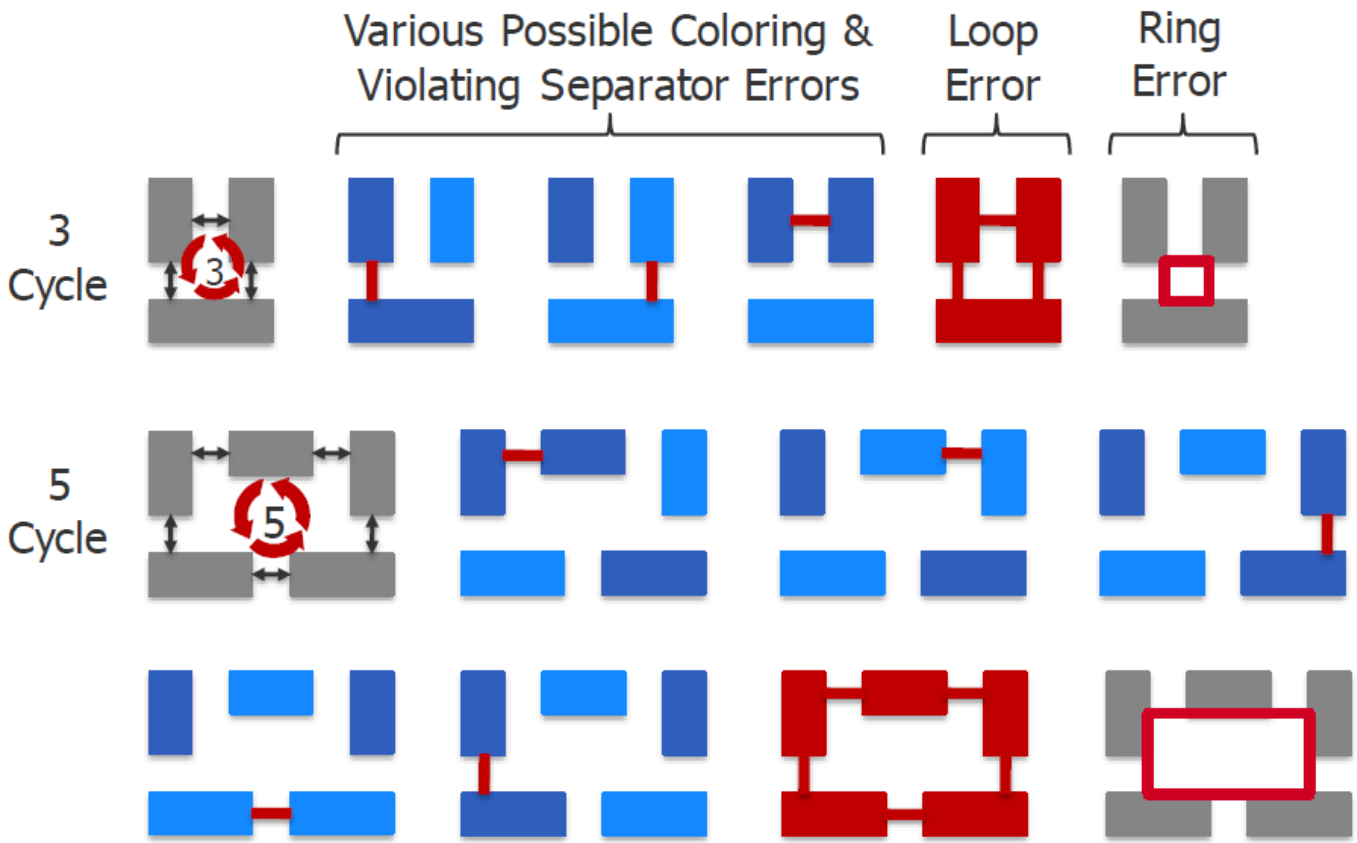
- DP handling varies from one foundry to the other.
- Some foundries makes it user transparent.
- Others make the user participate in coloring.



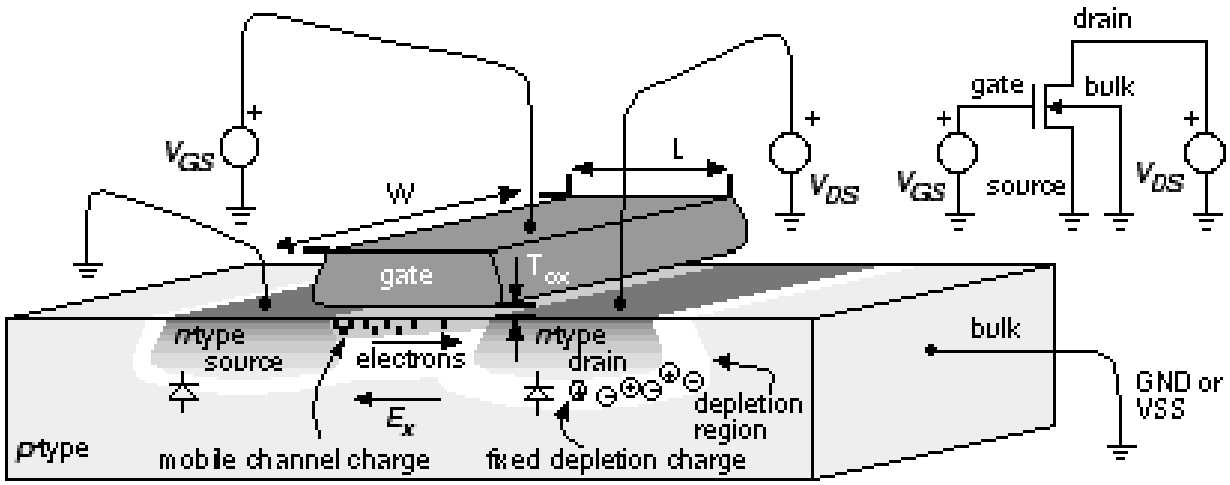
Example DP Decomposition Mask Output



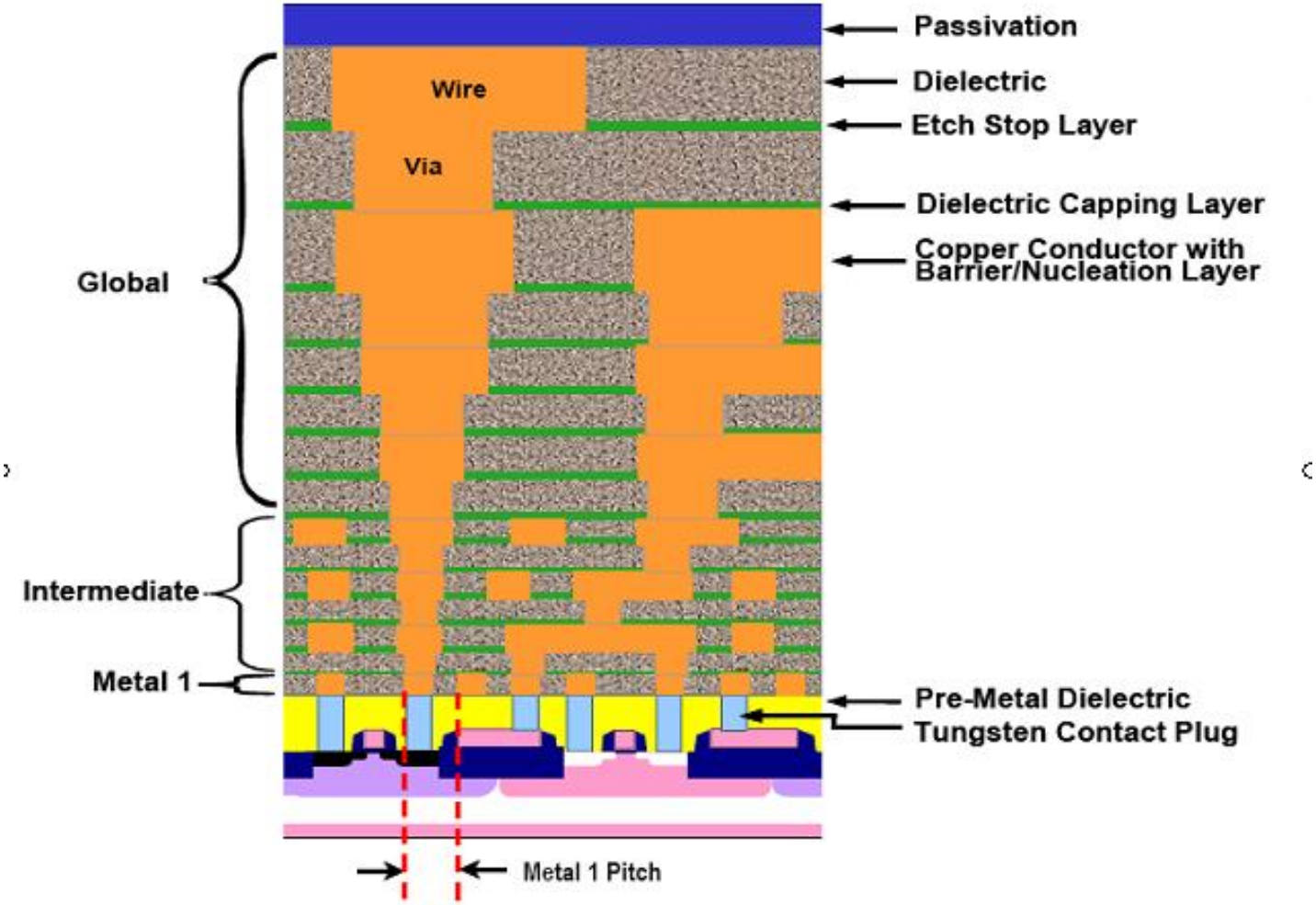
DP Violations (Odd Cycles)



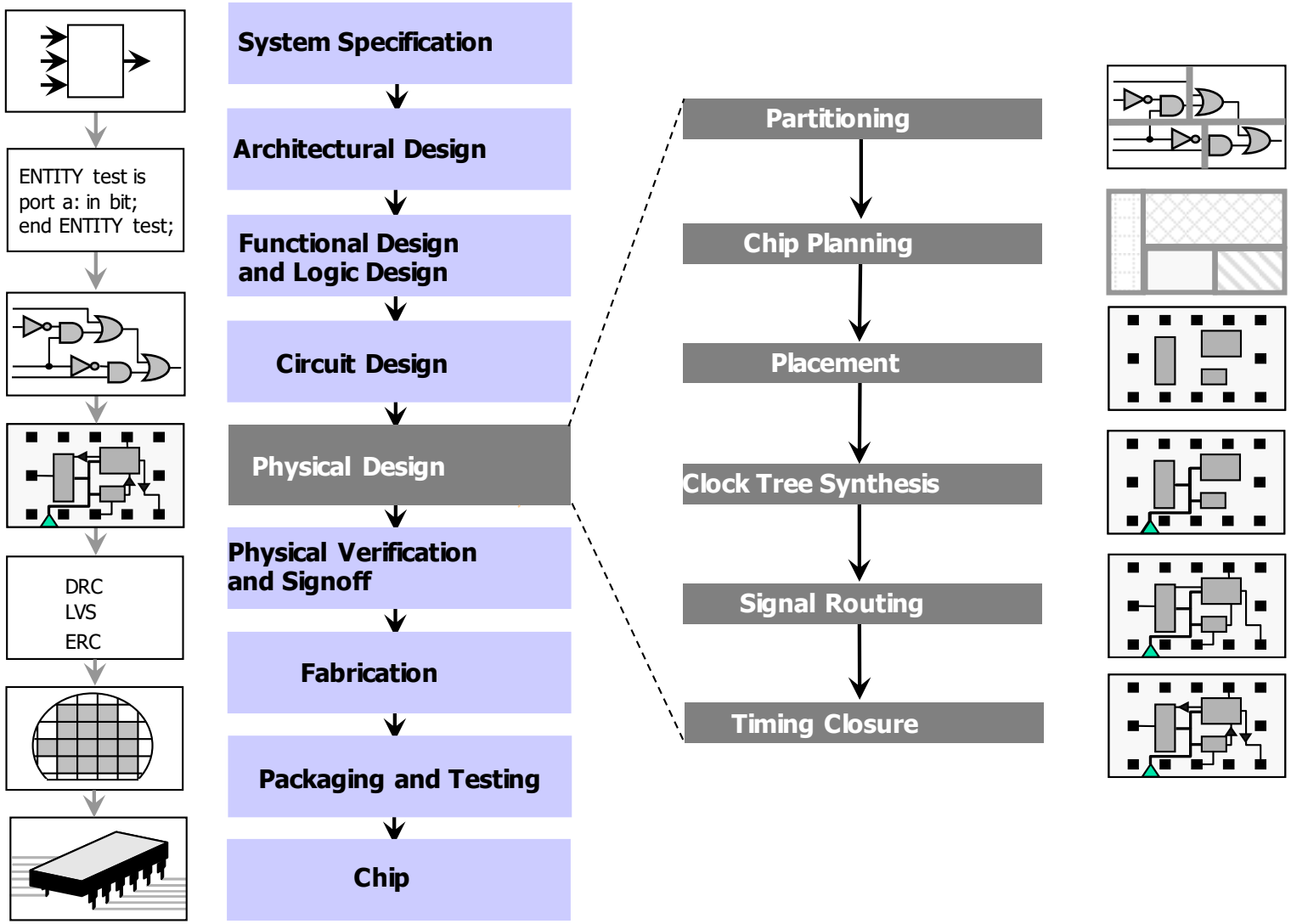
N-канальный МОП-транзистор



Топология СБИС в разрезе



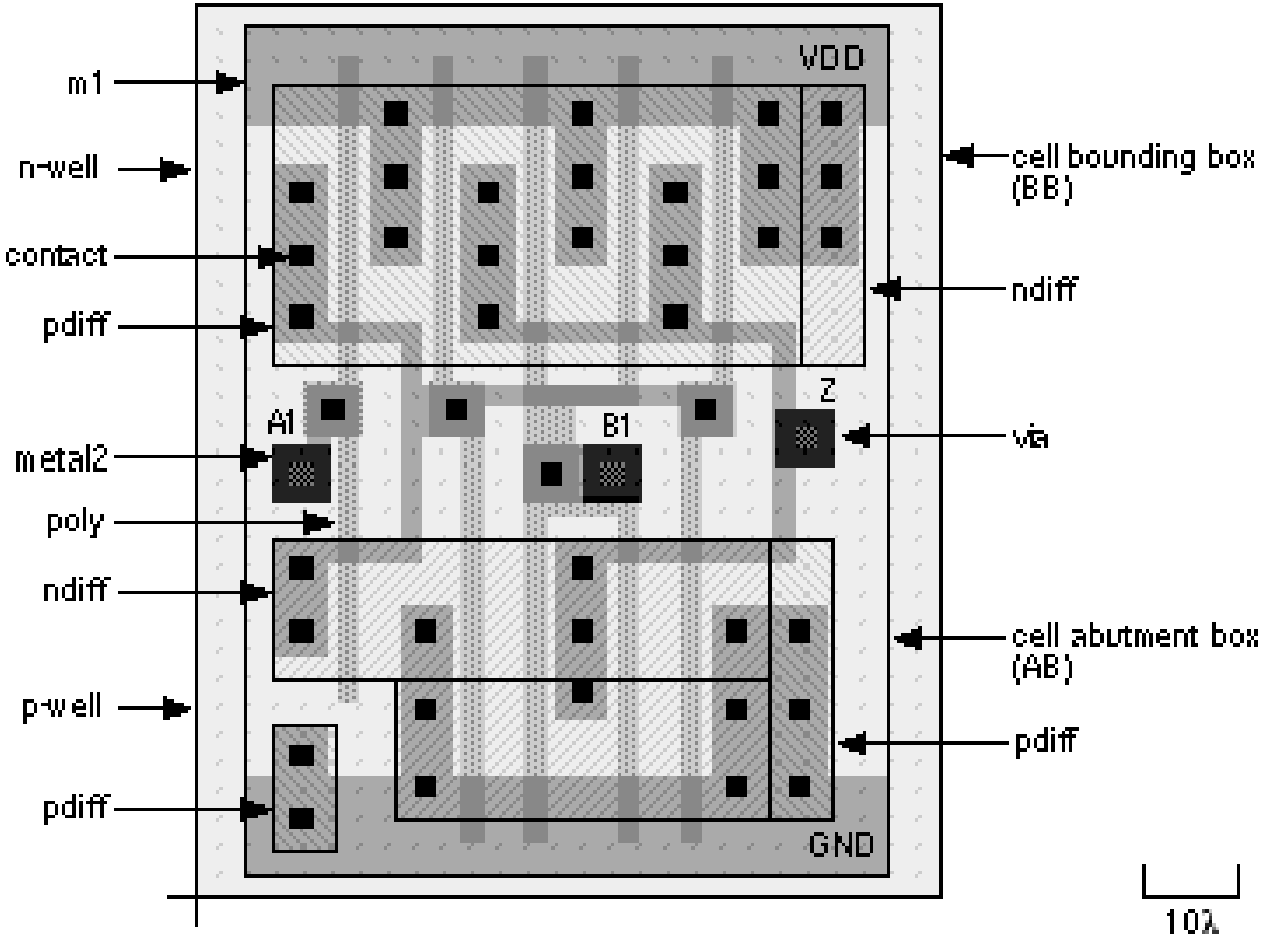
Маршрут проектирования СБИС



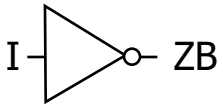
Стили проектирования

- Метод стандартных ячеек
- Заказное проектирование
- Программируемые логические массивы

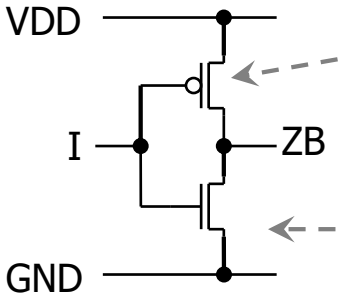
Топология стандартной ячейки

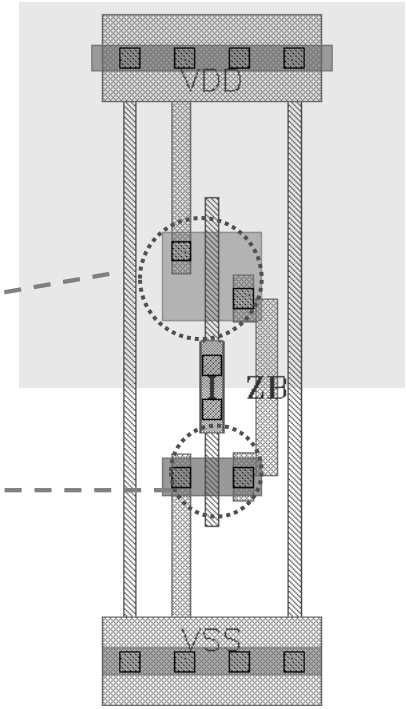


Инвертор

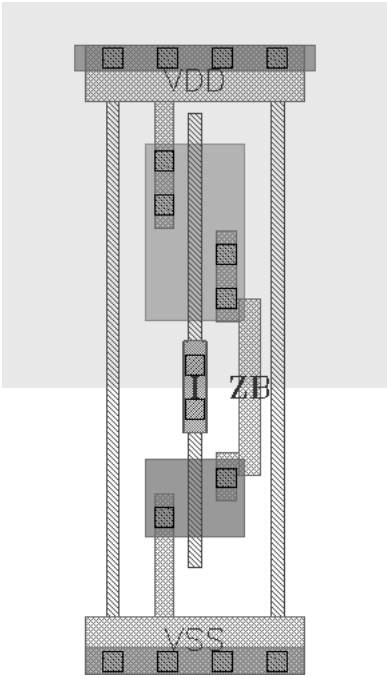


Инвертор		
I	0	1
ZB	1	0

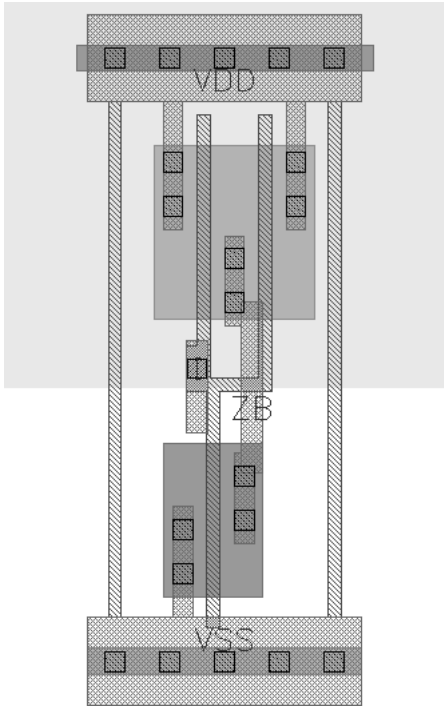




65 nm, standard fanout

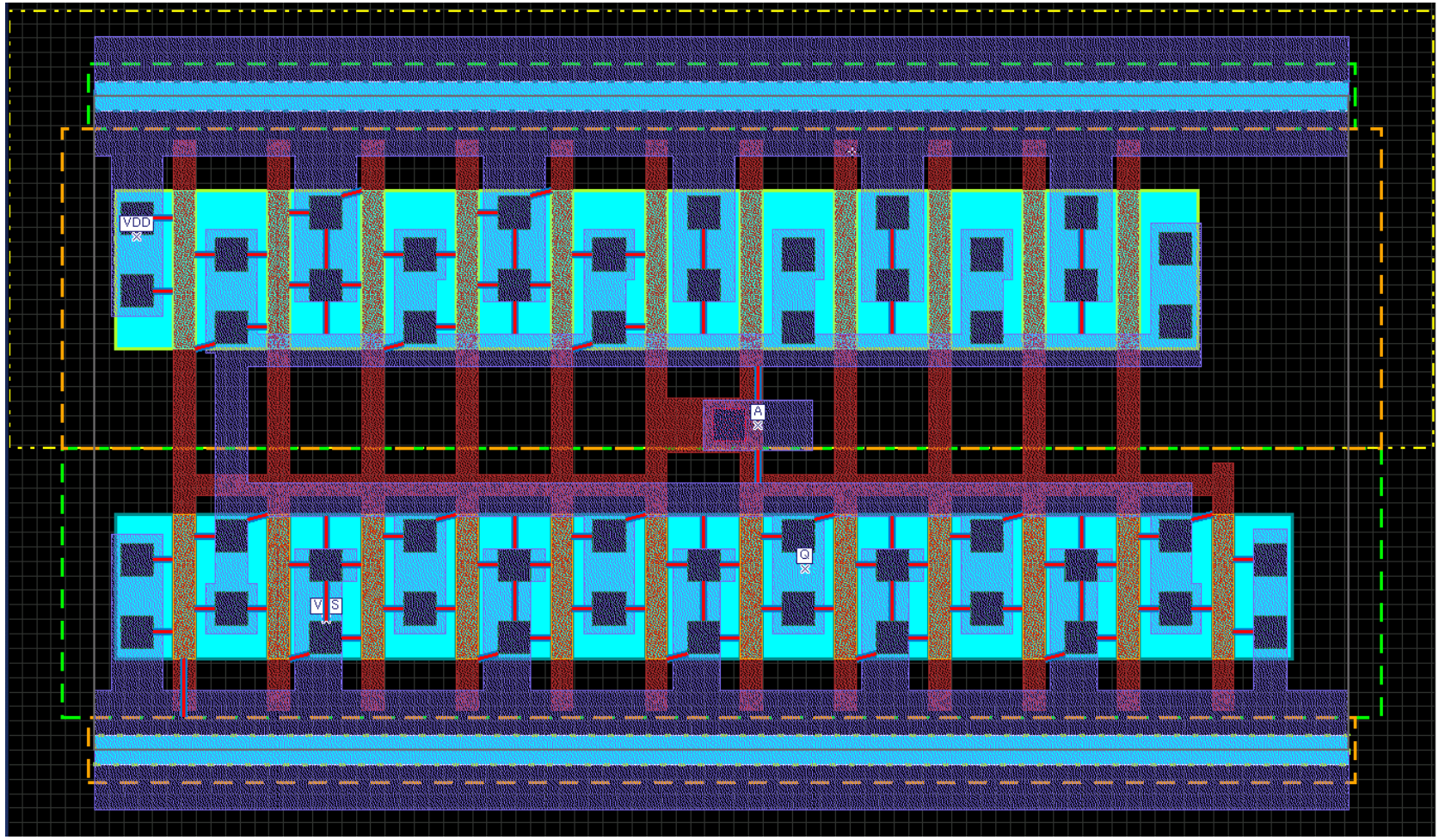


2x standard fanout

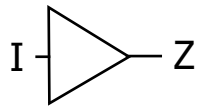


4x standard fanout

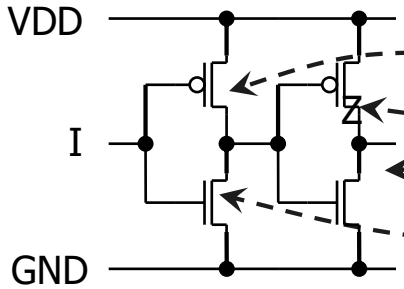
Топология инвертора 28 нм

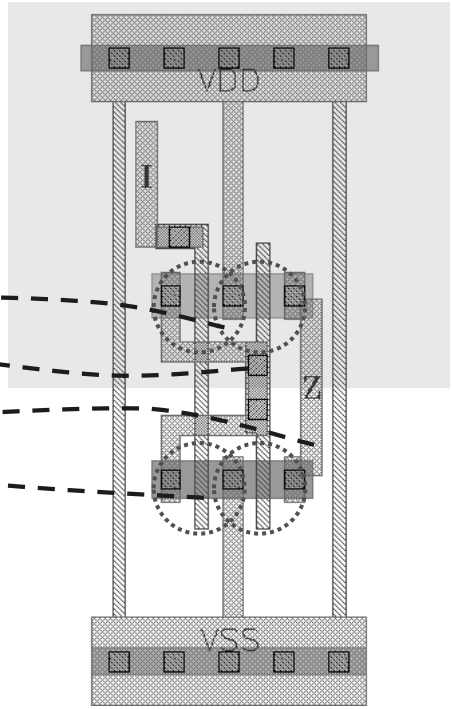


Буфер

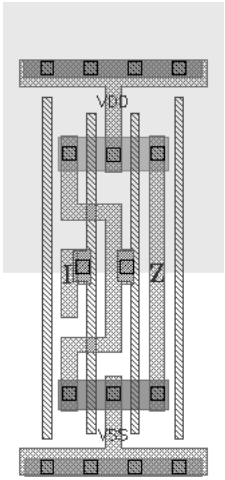


Буфер		
I	0	1
Z	0	1

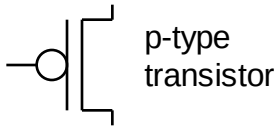




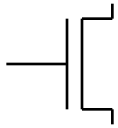
65 nm



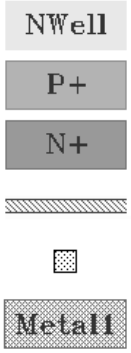
40 nm



p-type transistor



n-type transistor



n-well

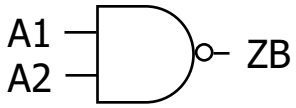
p/n diffusion

polysilicon

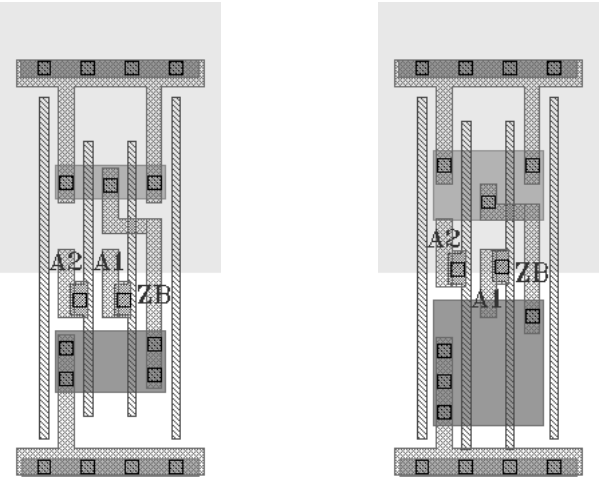
contact

metal layer 1

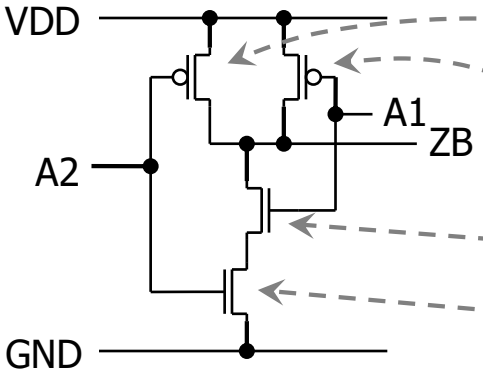
И-НЕ NAND gate (2-input)

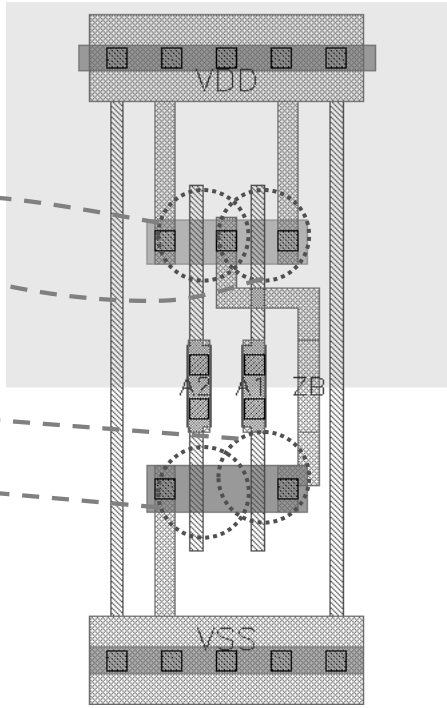


NAND				
A1	0	0	1	1
A2	0	1	0	1
ZB	1	1	1	0

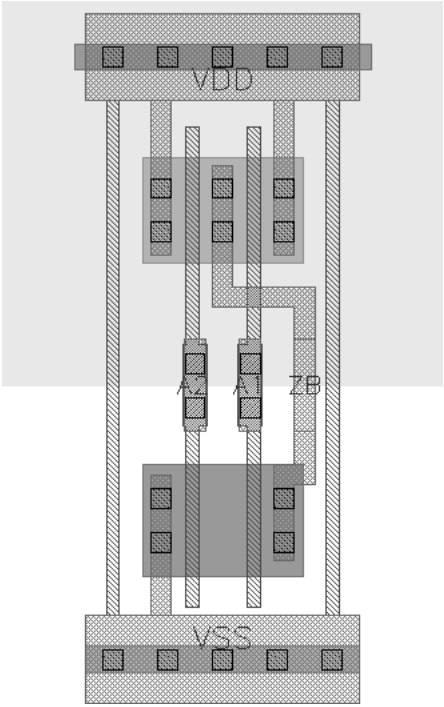


40 nm, 1x and 2x standard fanout



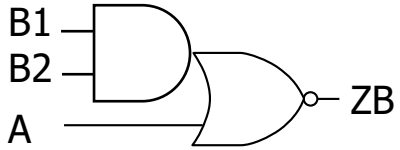


65 nm, standard fanout

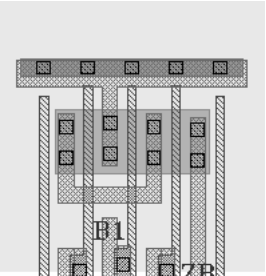


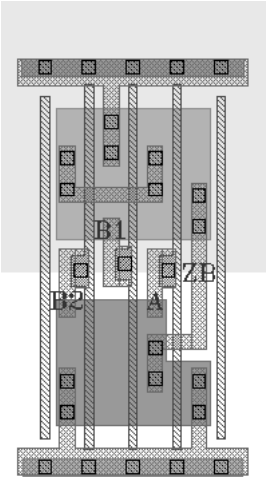
65 nm, 2x standard fanout

AND-OR-Invert (AOI) gate (2-1)

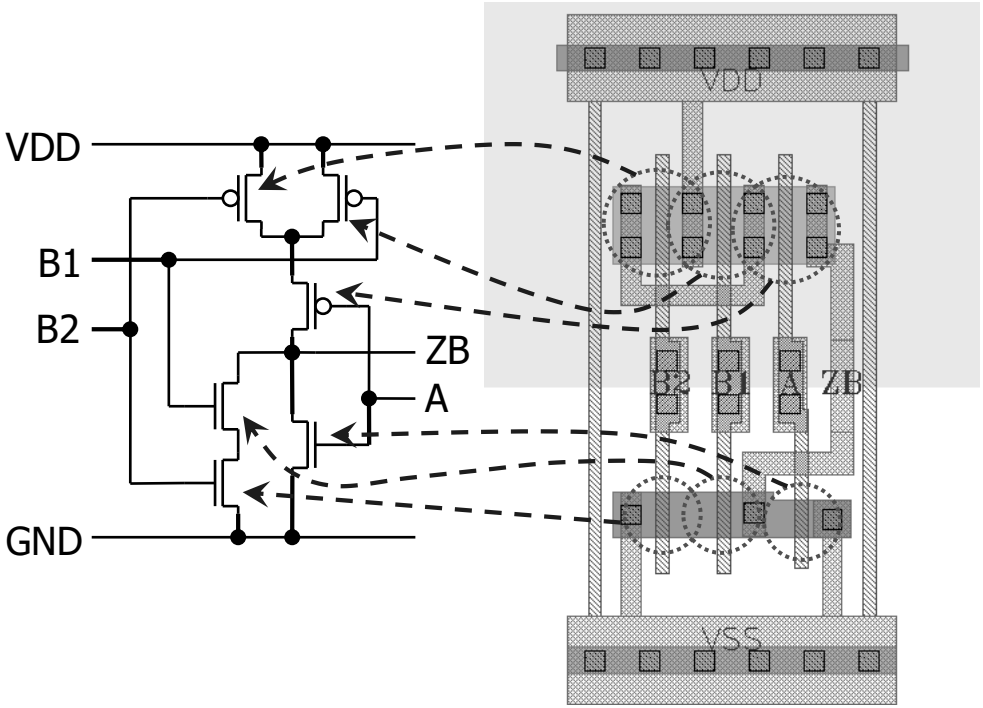


AOI								
A	0	0	0	0	1	1	1	1
B1	0	0	1	1	0	0	1	1
B2	0	1	0	1	0	1	0	1
ZB	1	1	1	0	0	0	0	0

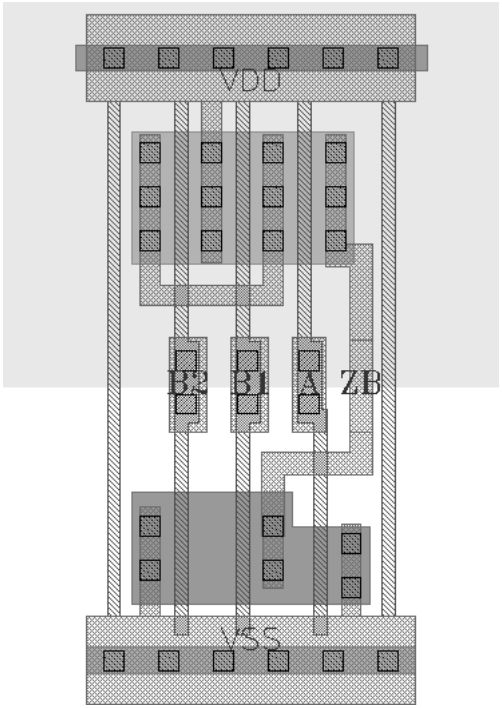




40 nm, 1x and 2x standard fanout

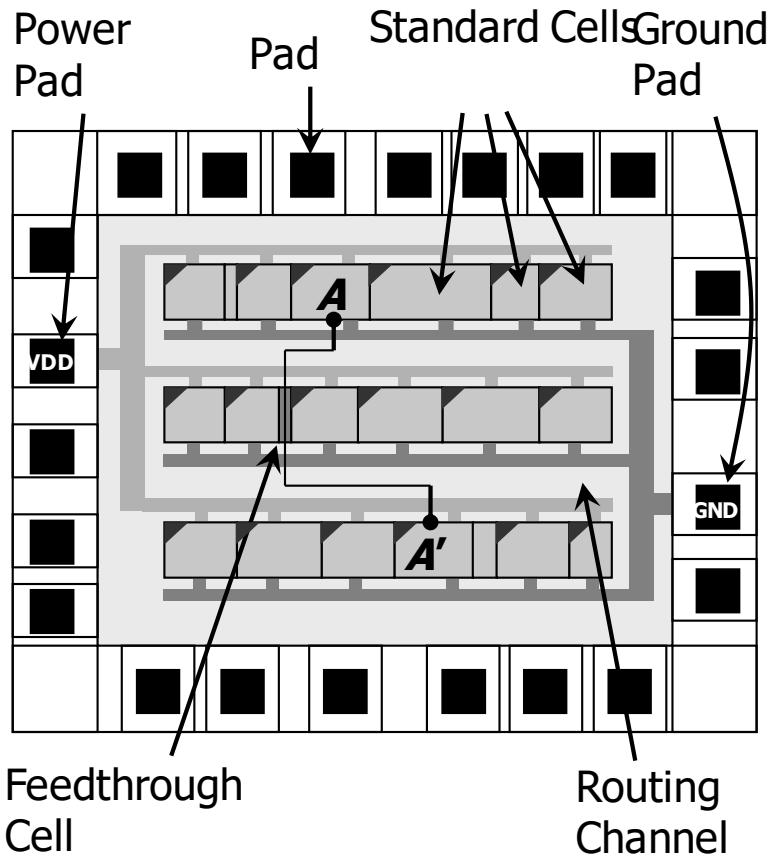


65 nm, standard fanout

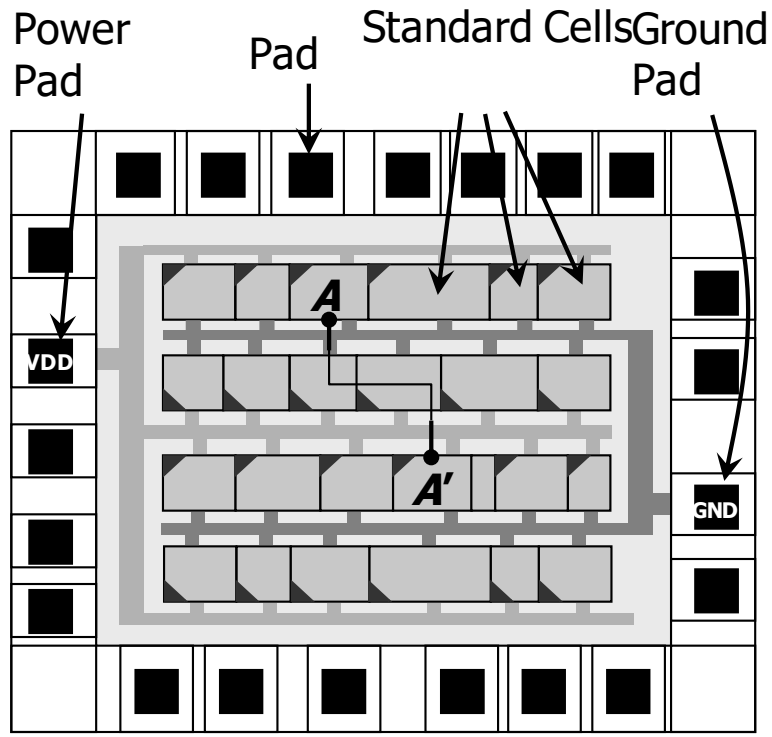


65 nm, 2x standard fanout

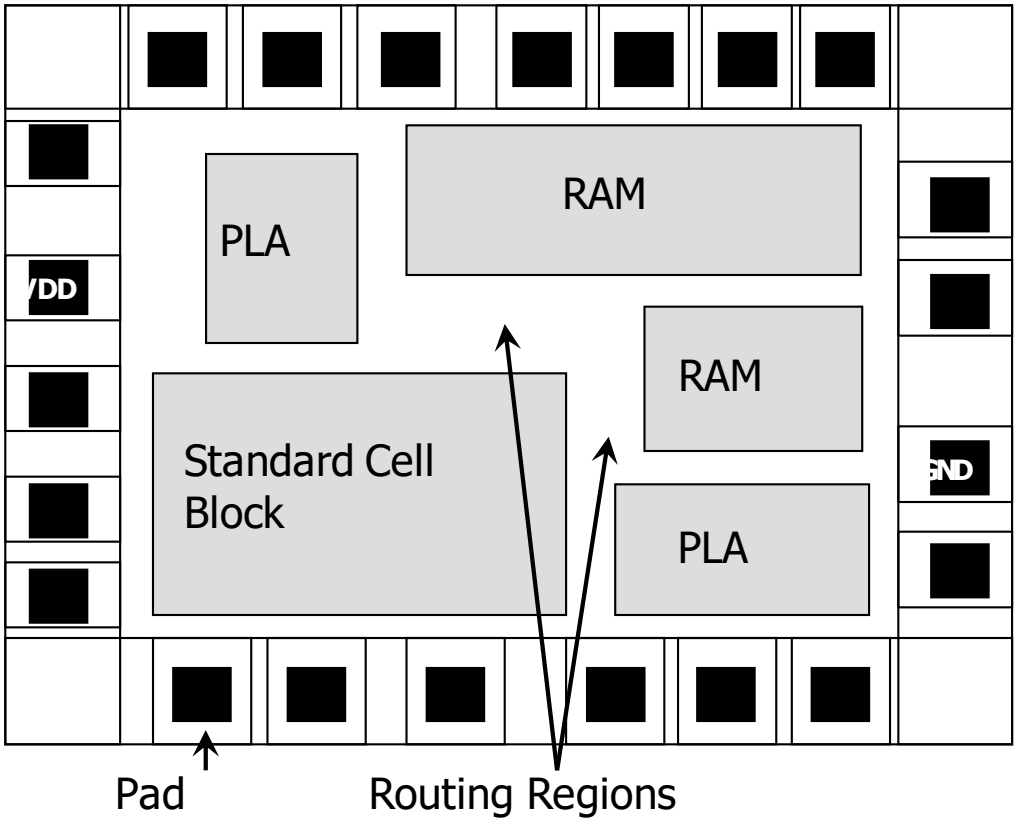
Standard cell layout with a feedthrough cell



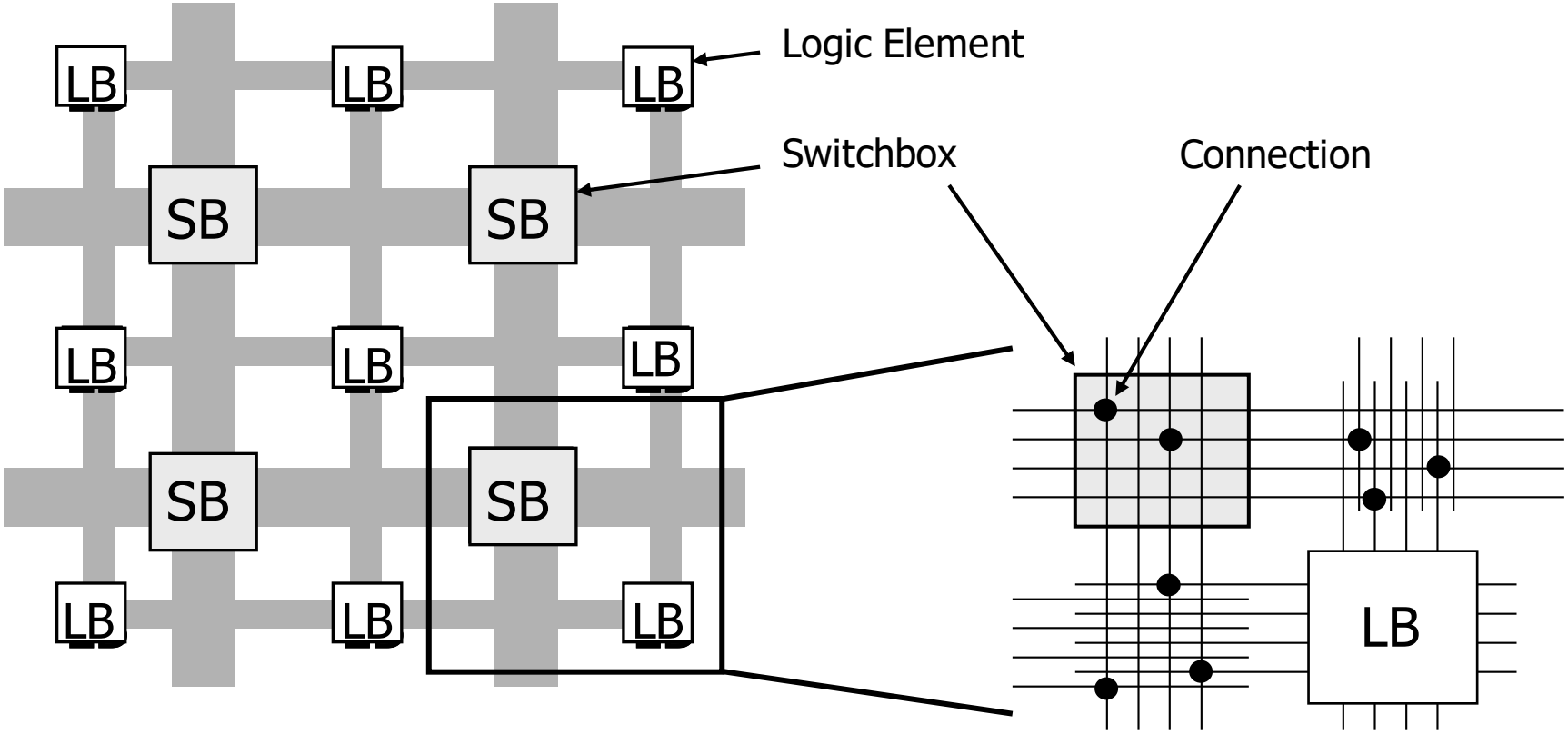
Standard cell layout using over-the-cell (OTC routing



Layout with macro cells



Field-programmable gate array (FPGA) (ПЛМ)



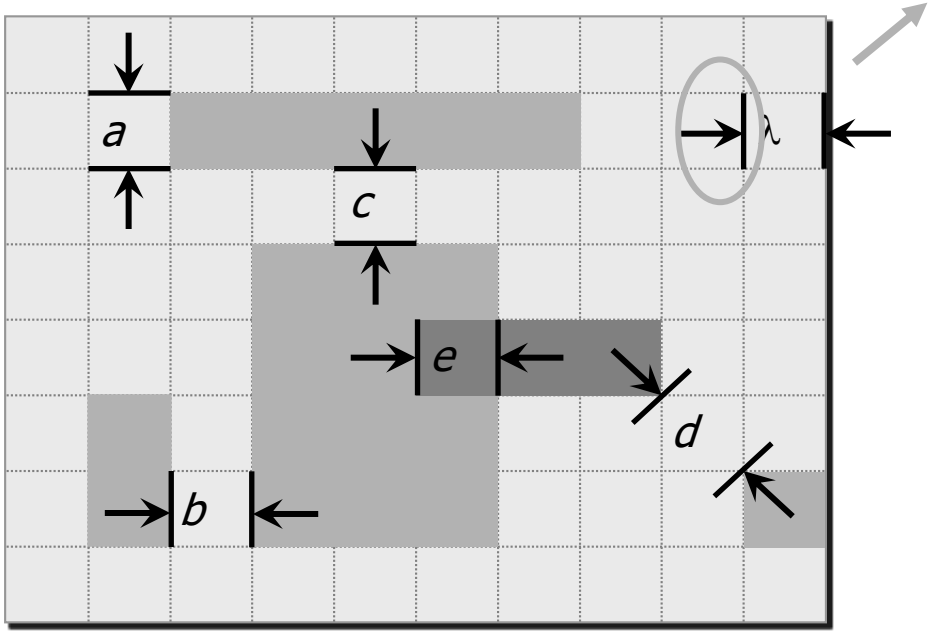
Типы правил проектирования (Design Rules)

- Size rules, such as *minimum width*: The dimensions of any component (shape), e.g., length of a boundary edge or area of the shape, cannot be smaller than given minimum values. These values vary across different metal layers.

- Separation rules, such as *minimum separation*: Two shapes, either on the same layer or on adjacent layers, must be a minimum (rectilinear or Euclidean diagonal) distance apart.

- Overlap rules, such as *minimum overlap*: Two connected shapes on adjacent layers must have a certain amount of overlap due to inaccuracy of mask alignment to previously-made patterns on the wafer.

Типы правил проектирования (Design Rules)



λ: smallest meaningful technology-dependent unit of length

Minimum Width: *a*

Minimum Separation: *b*, *c*, *d*

Minimum Overlap: *e*

Типы ограничений (constraints)

- Technology constraints enable fabrication for a specific technology node and are derived from technology restrictions. Examples include minimum layout widths and spacing values between layout shapes.

- Electrical constraints ensure the desired electrical behavior of the design. Examples include meeting maximum timing constraints for signal delay and staying below maximum coupling capacitances.

- Geometry (design methodology) constraints are introduced to reduce the overall complexity of the design process. Examples include the use of preferred wiring directions during routing, and the placement of standard cells in rows.

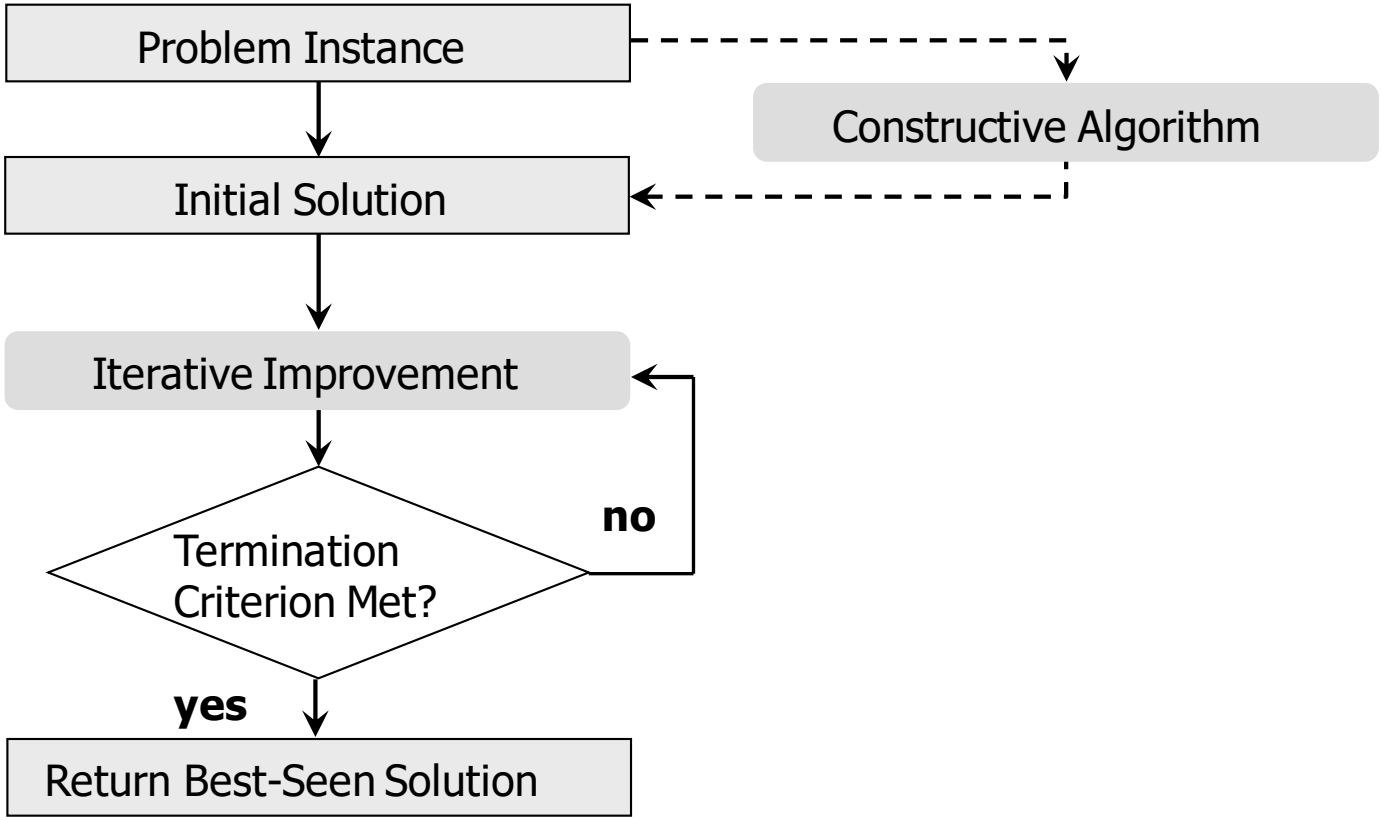
Эвристические алгоритмы

- Deterministic: All decisions made by the algorithm are repeatable, i.e., not random. One example of a deterministic heuristic is Dijkstra's shortest path algorithm.

- Stochastic: Some decisions made by the algorithm are made randomly, e.g., using a pseudo-random number generator. Thus, two independent runs of the algorithm will produce two different solutions with high probability. One example of a stochastic algorithm is simulated annealing.

- In terms of structure, a heuristic algorithm can be
  - Constructive: The heuristic starts with an initial, incomplete (partial) solution and adds components until a complete solution is obtained.
  - Iterative: The heuristic starts with a complete solution and repeatedly improves the current solution until a preset termination criterion is reached.

Эвристические алгоритмы



Этапы развития САПР СБИС

Time Period	Circuit and Physical Design Process Advancements
1950 -1965	Manual design only.
1965 -1975	Layout editors, e.g., place and route tools, first developed for printed circuit boards.
1975 -1985	More advanced tools for ICs and PCBs, with more sophisticated algorithms.
1985 -1990	First performance-driven tools and parallel optimization algorithms for layout; better understanding of underlying theory (graph theory, solution complexity, etc.).
1990 -2000	First over-the-cell routing, first 3D and multilayer placement and routing techniques developed. Automated circuit synthesis and routability-oriented design become dominant. Start of parallelizing workloads. Emergence of physical synthesis.
2000 - now	Design for Manufacturability (DFM), optical proximity correction (OPC), and other techniques emerge at the design-manufacturing interface. Increased reusability of blocks, including intellectual property (IP) blocks.